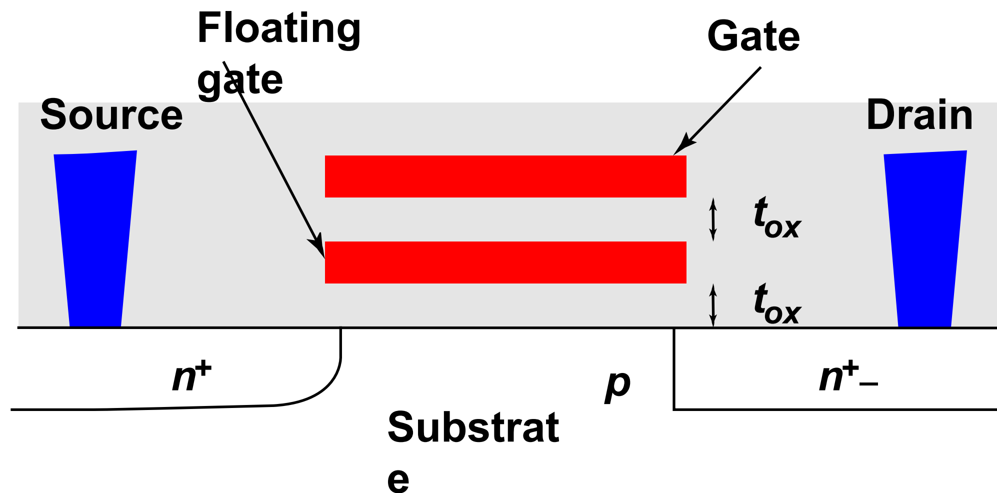
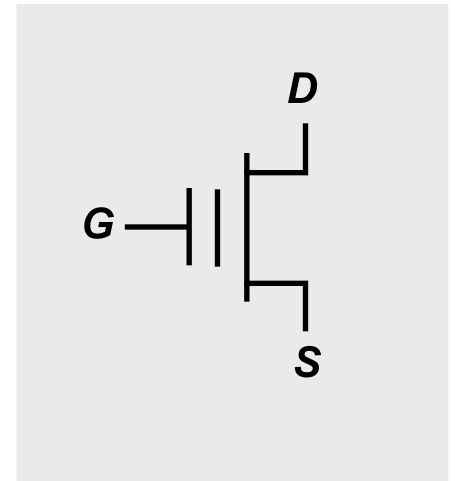
CSE 122/222
Non-Volatile Memory

Non-Volatile Memories
The Floating-gate transistor

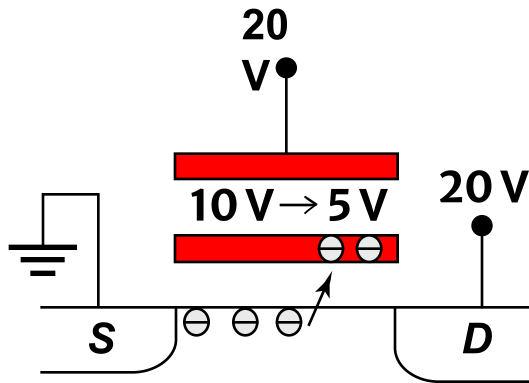


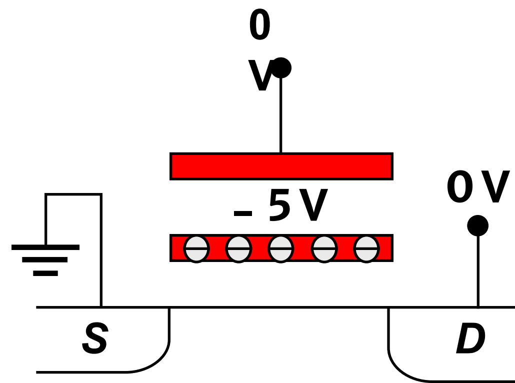
Device
cross-section

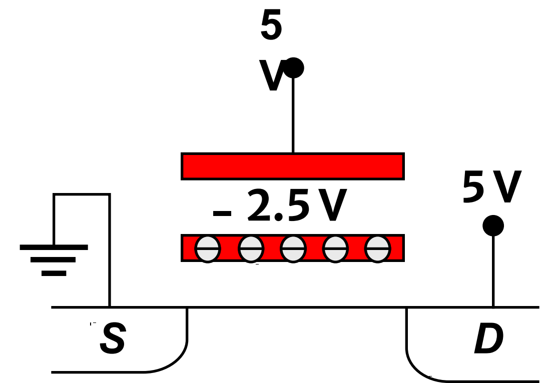


Schematic symbol

Floating-Gate Transistor Programming





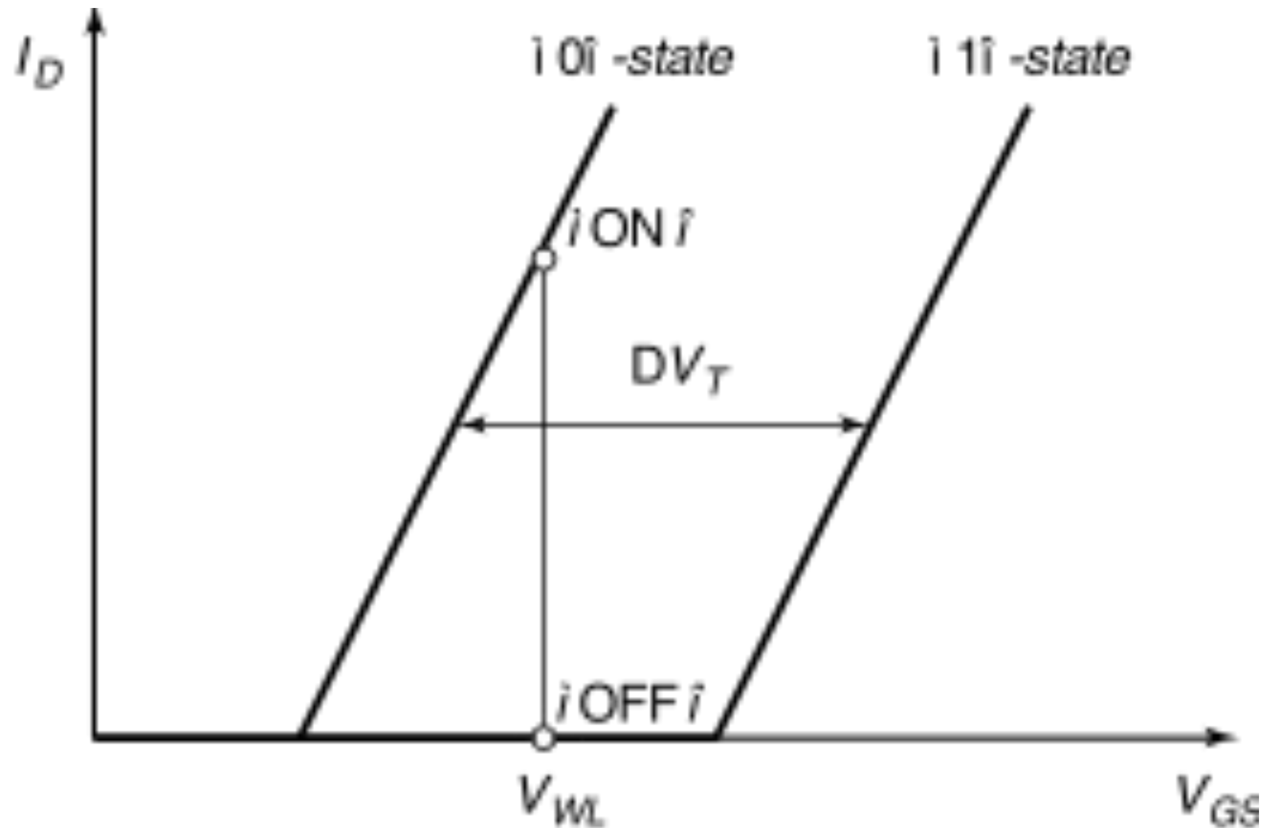


Avalanche injection

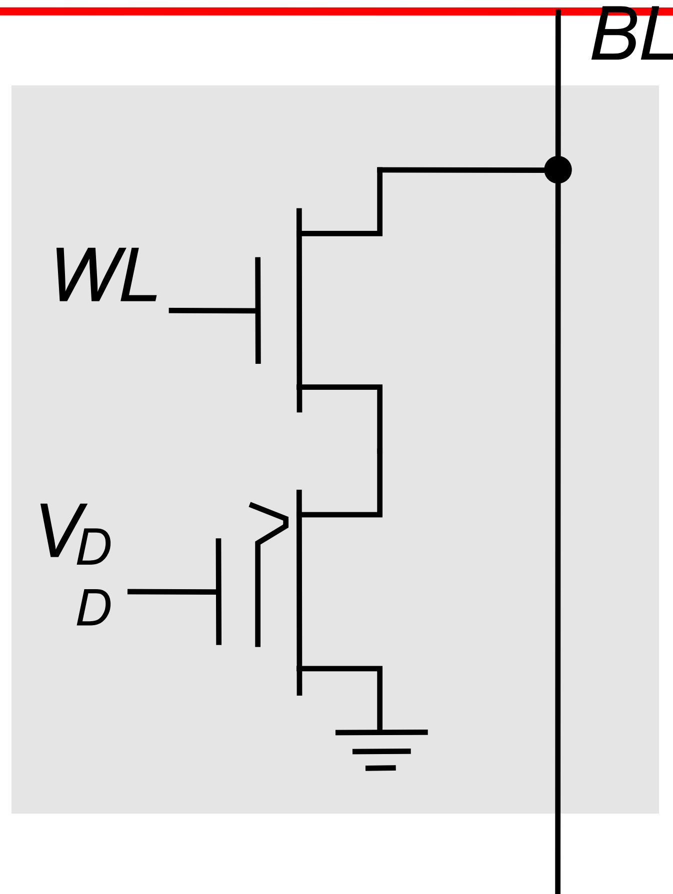
Removing programming voltage leaves charge trapped

Programming results in higher V_T.

A “Programmable-Threshold” Transistor

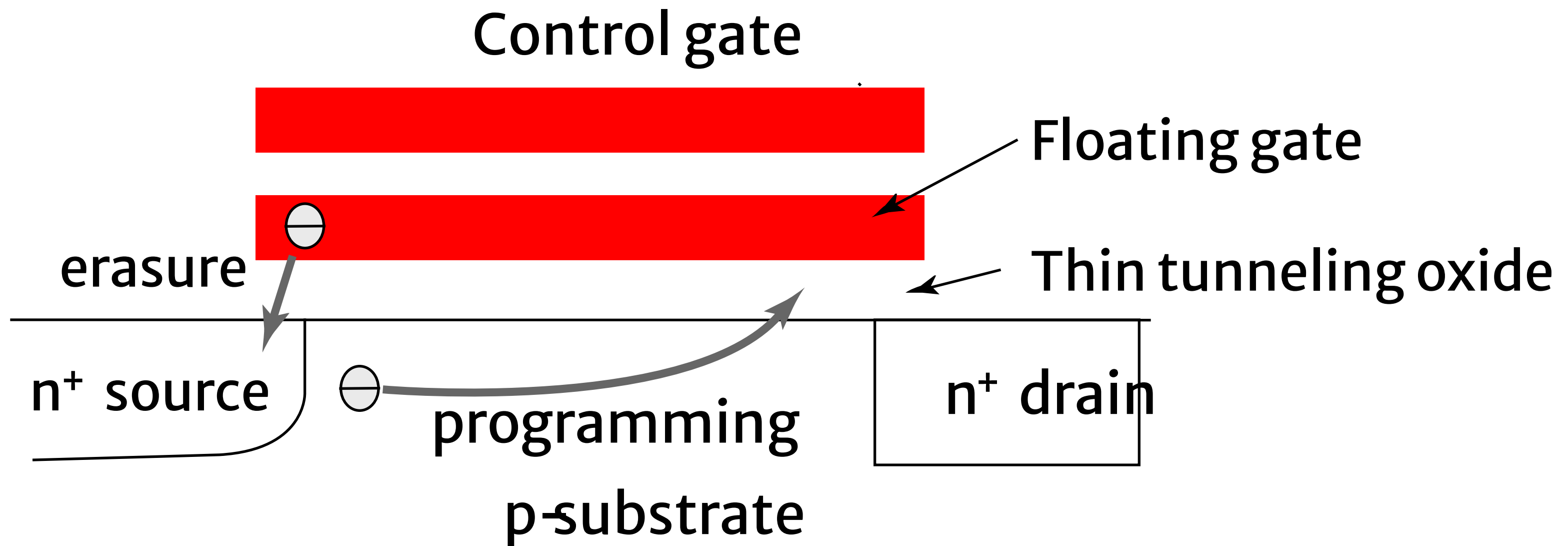


EEPROM Cell



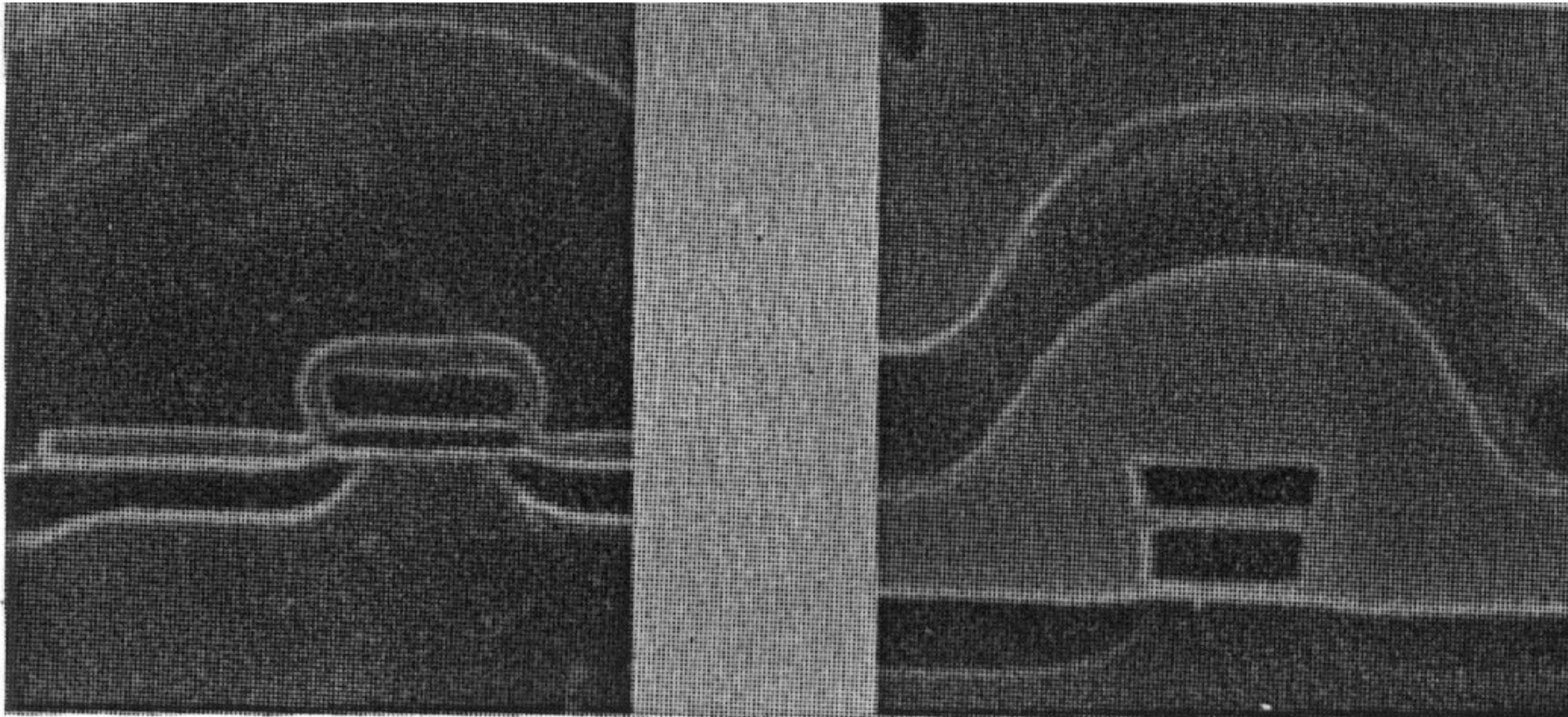
Absolute threshold control is hard
Unprogrammed transistor might be depletion
⇨ **2 transistor cell**

Flash EEPROM



Many other options …

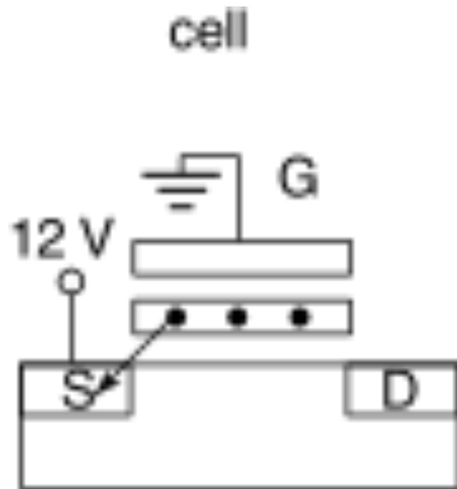
Cross-sections of NVM cells

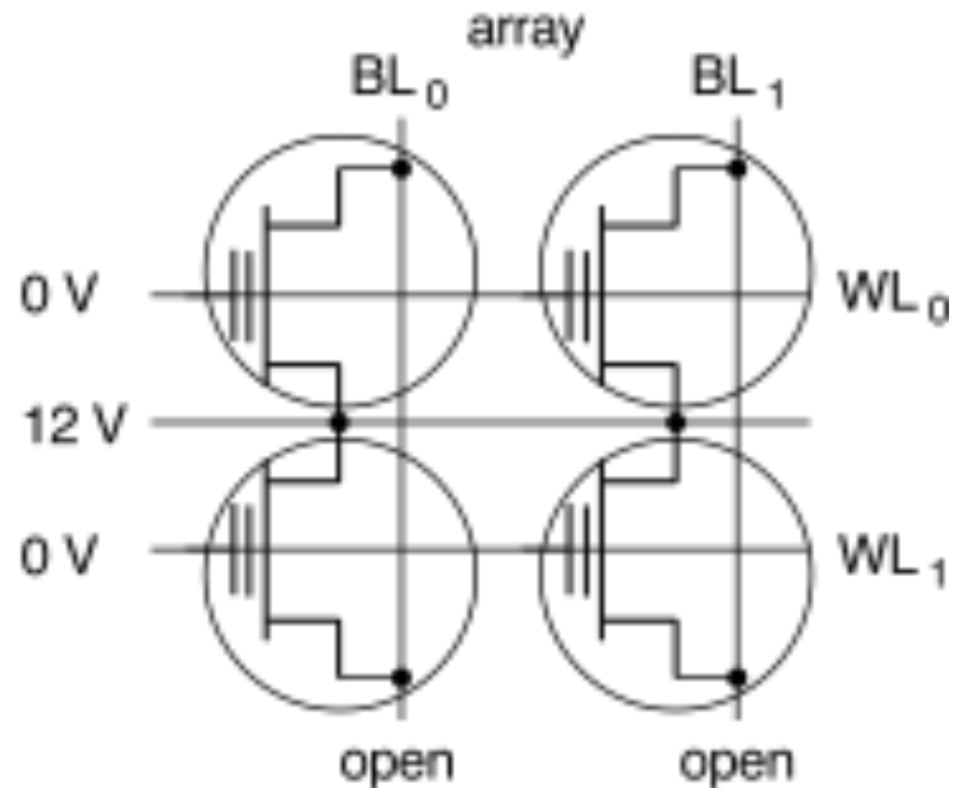


Flash **EPROM**

Courtesy Intel

Basic Operations in a NOR Flash Memory—Erase



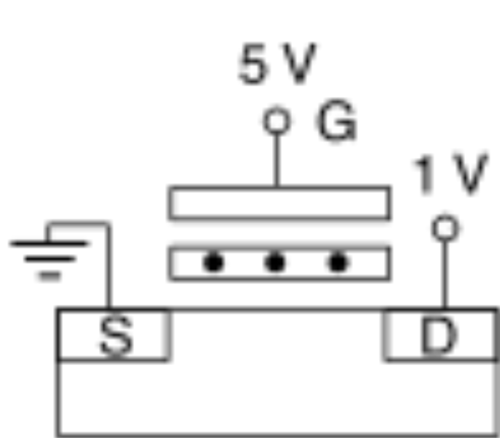


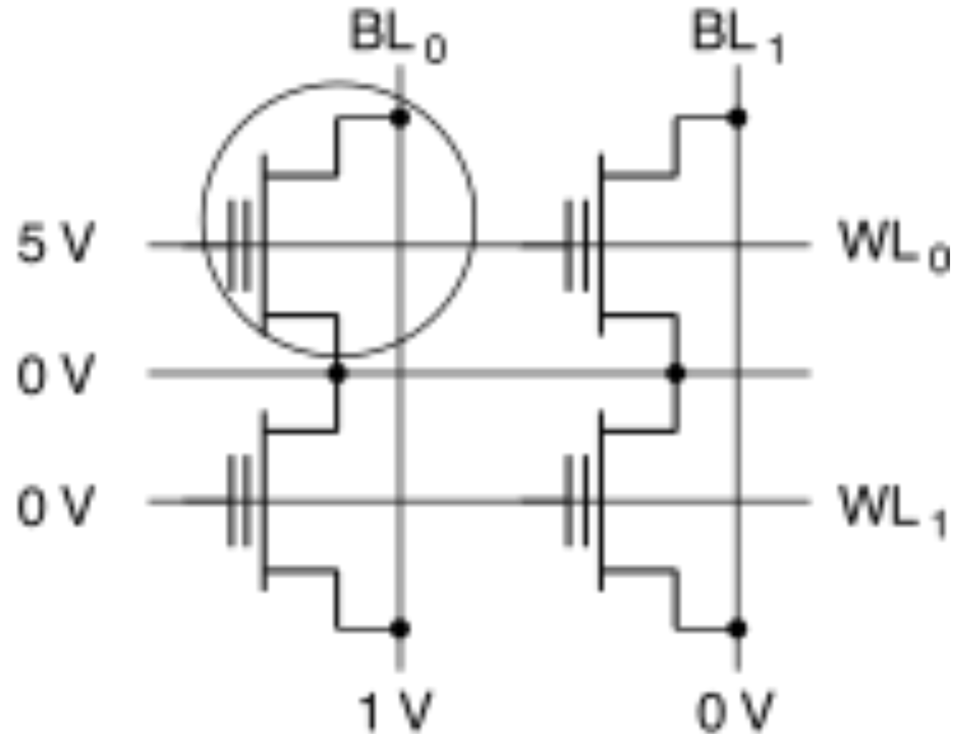
Basic Operations in a NOR Flash Memory—Write

12 V
G
6 V
S
D

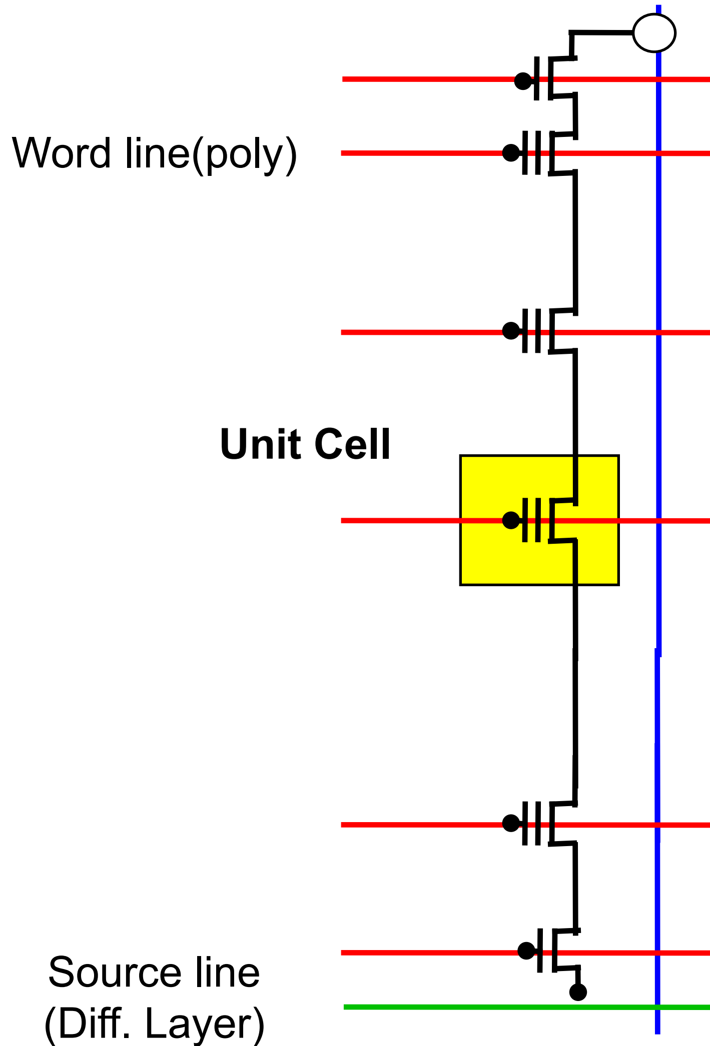
BL 0
BL 1
12 V
WL 0
0 V
0 V
WL 1
6 V
0 V

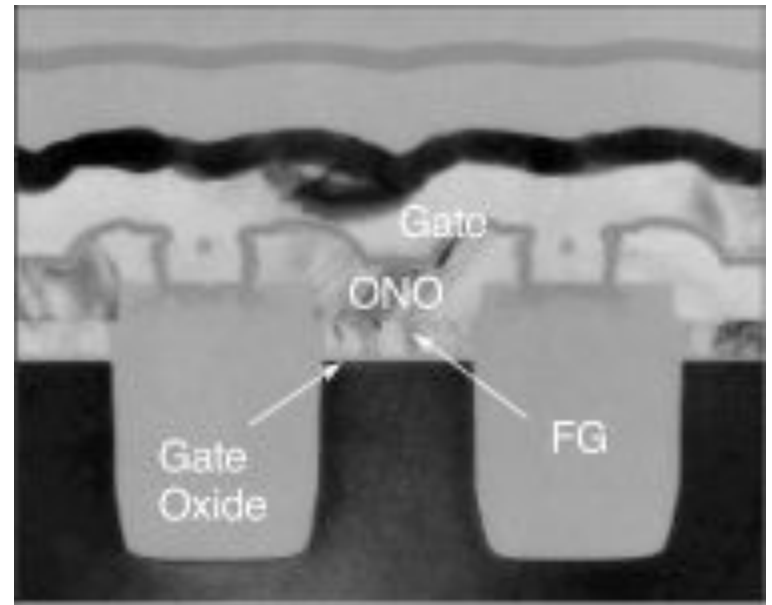
Basic Operations in a NOR Flash Memory—Read





NAND Flash Memory





Courtesy Toshiba

NAND Flash Memory

Select transistor

Word lines

Active area

STI

Bit line contact

Source line contact

Courtesy Toshiba

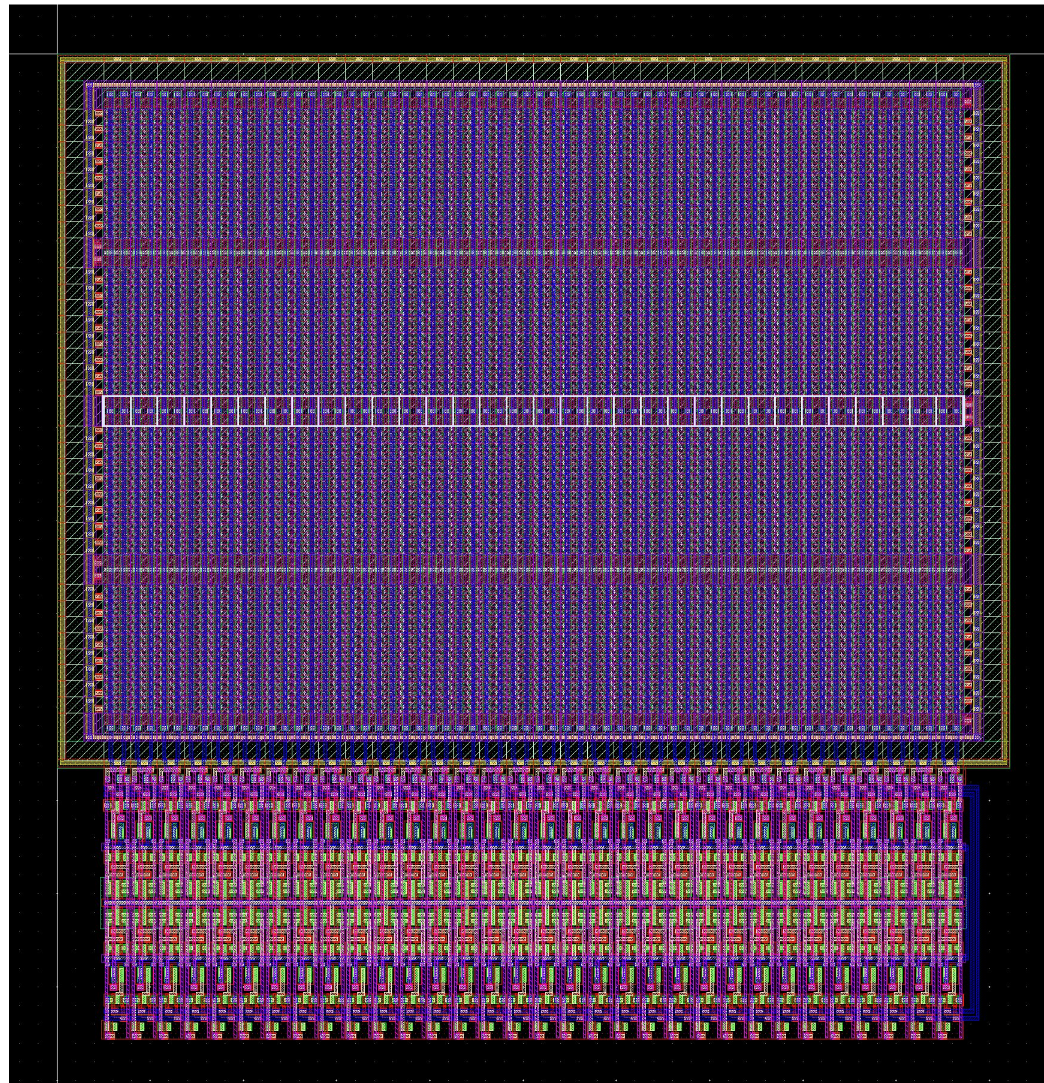
NAND Flash READ

- Pull n-1 bit lines above programmed Vth to turn them on
- One pulled above Vth of an erased bit
- Will pull down iff selected bit has NOT been programmed

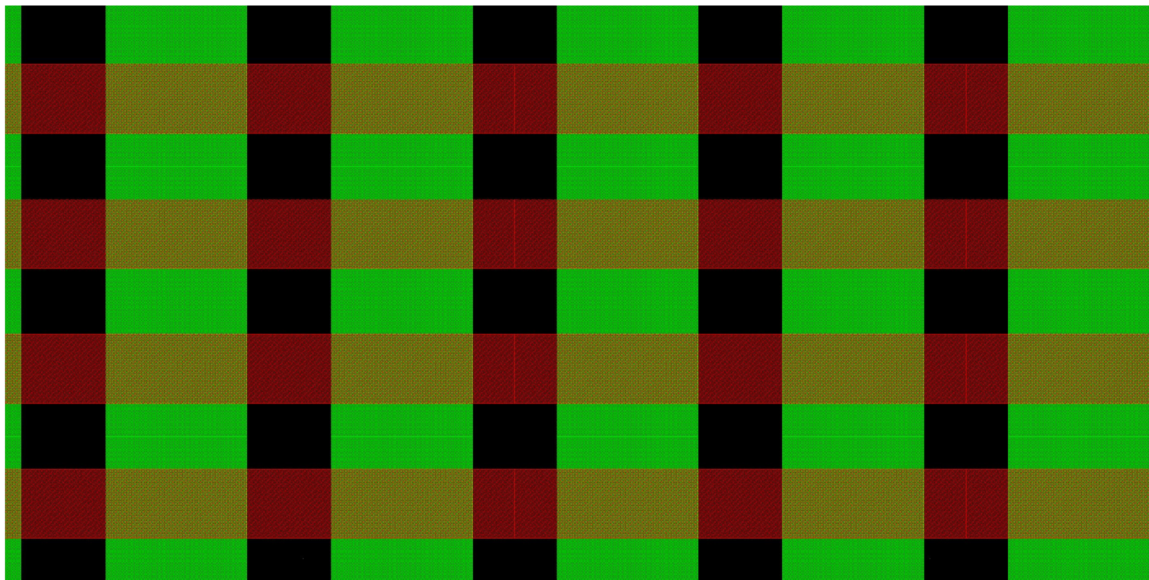
NAND Flash WRITE/ERASE

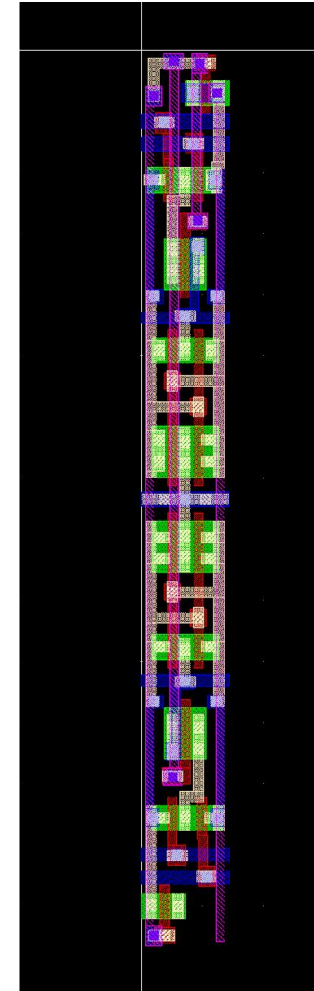
- ERASE sets all bits to 1
  - Charges floating gates (Vg=0V, Vs=12V)
- WRITE can only set bits to 0
  - Discharges floating gates (Vg=12V,Vd=6V)
- Can WRITE as long as 0's are subset of 1's
    - Ex. Write 1111 then 1110 then 1010 etc.
- External RAM needed to cache results during ERASE/WRITE

Sky130 64x64 Flash Array + Sense Amps

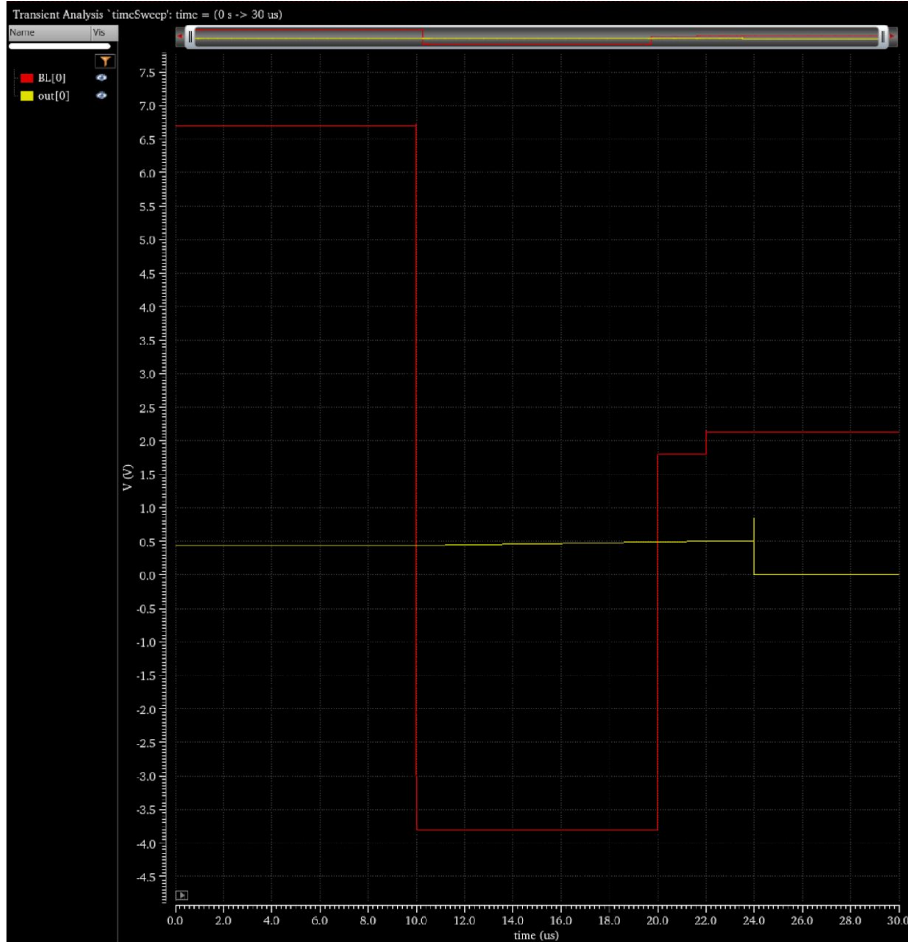


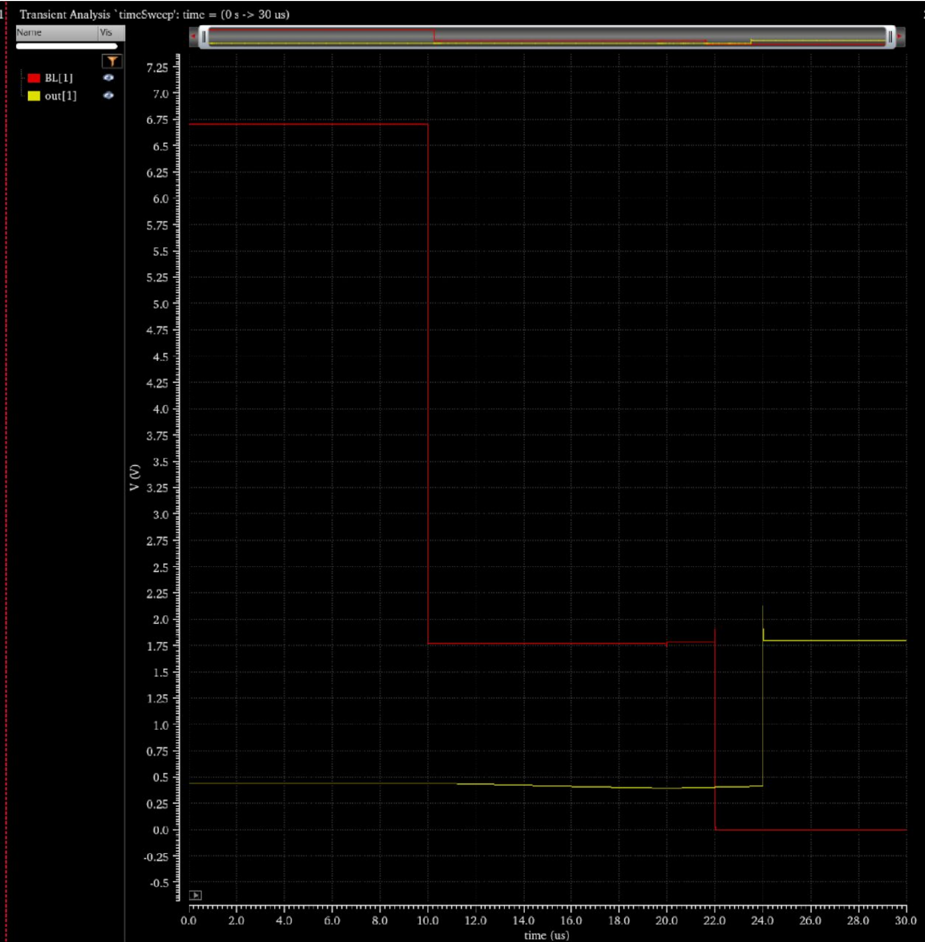
NAND Flash and Sense Amp





Left: Programmed, Right: Cleared

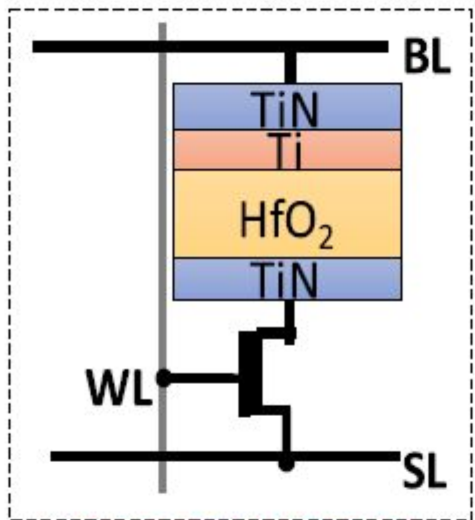


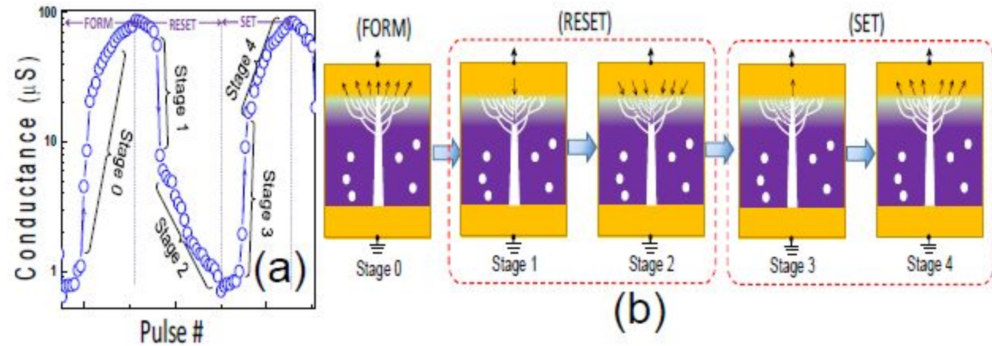


Wear Leveling

- Each programming of floating gate damages the oxide
  - Limited number of writes (10k-100k?)
- Wear leveling can remap frequently written addresses to “even out” wear
- Requires programmable address decoding
- Increases write lifetime to 100k-1M

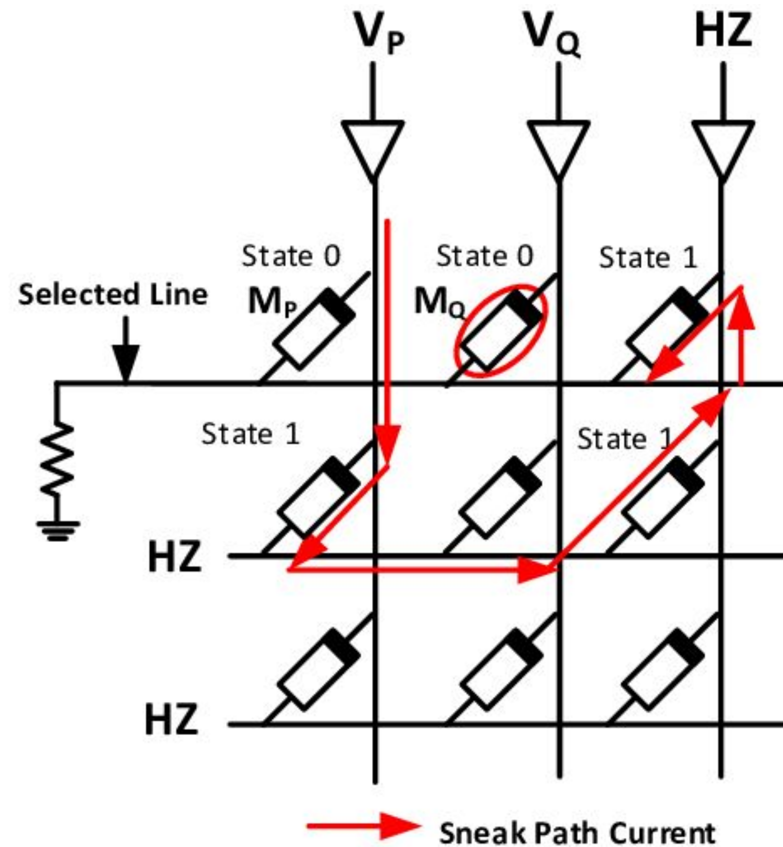
ReRAM





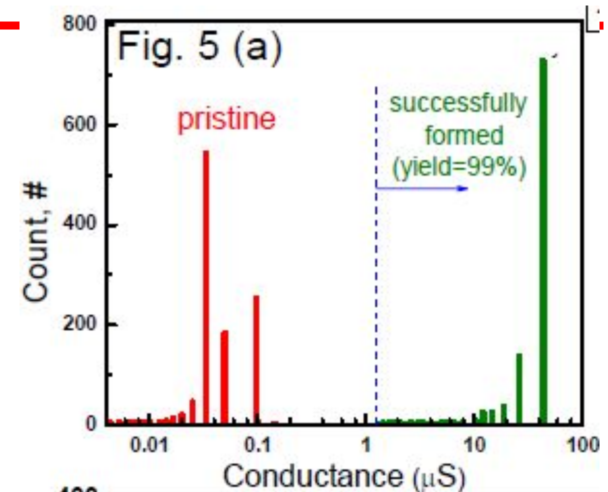
Hsieh et al, High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning

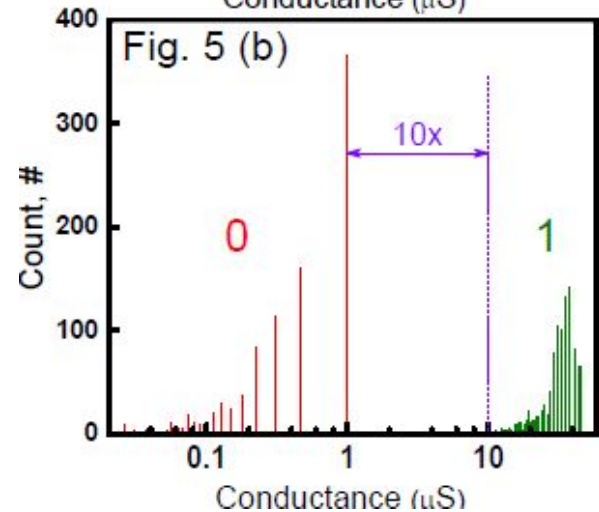
Sneak Paths in Crossbar Arrays



Form, Reset, and Set

1T1R #5	WL (V)	BL (V)	SL (V)	PW (ns)
Pristine				
Form	1.4 – 2.0 (0.1 step)	2.6 – 3.1 (0.1 step)	0	1000
Reset	2.5	0	2.6	1000
Set	1.7	2.4	0	1000

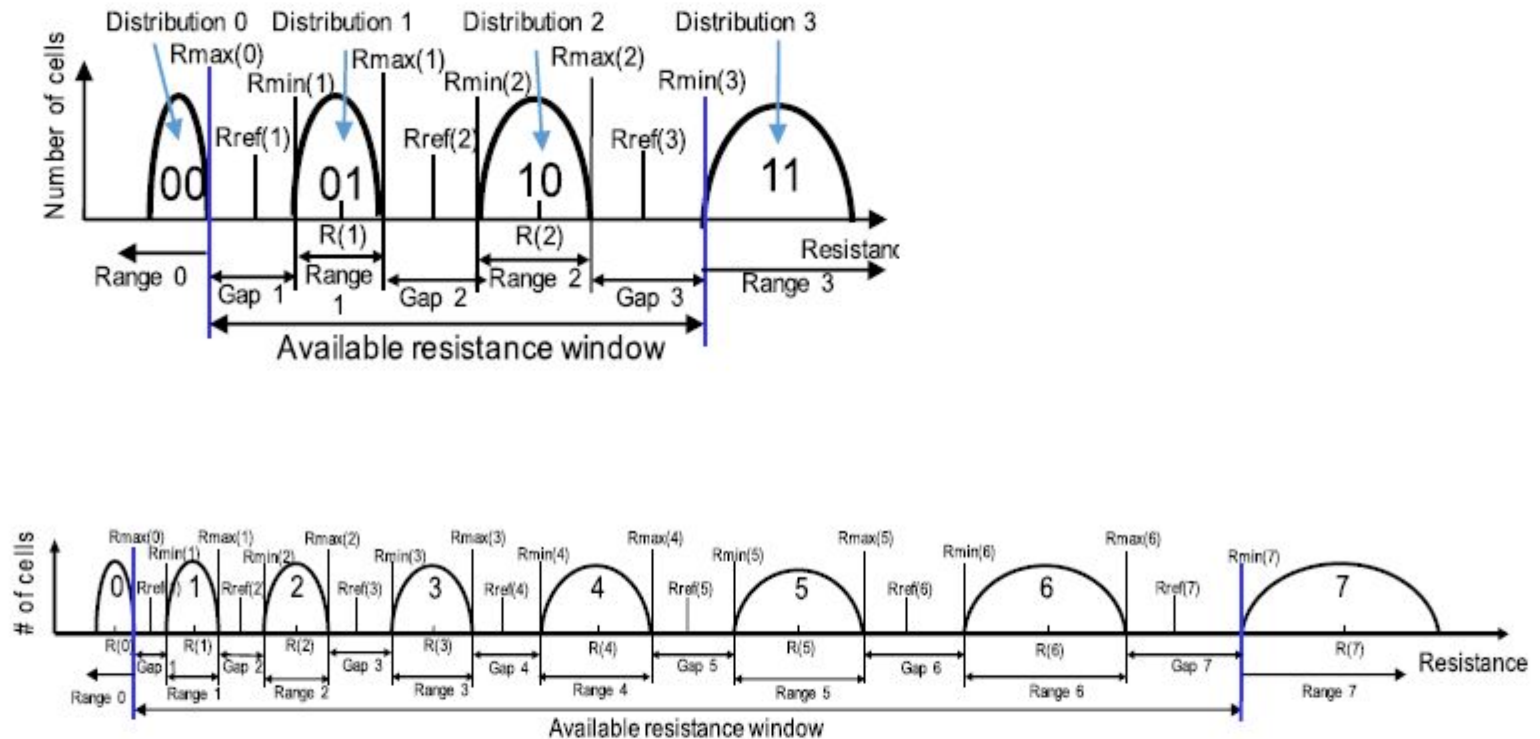




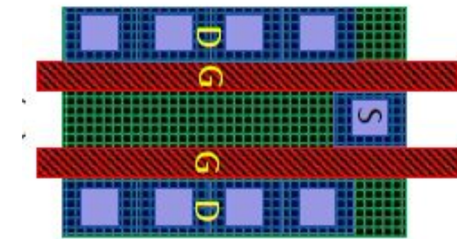
Le et al, Resistive RAM With Multiple Bits Per Cell: Array-Level Demonstration of 3 Bits Per Cell, IEEE Electron Devices, 2019.

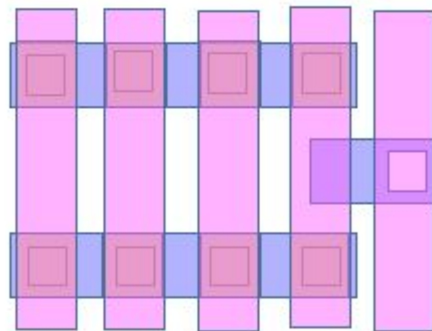
Hsieh et al, High-Density Multiple Bits-per-Cell 1T4R RRAM Array with Gradual SET/RESET and its Effectiveness for Deep Learning

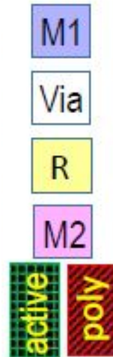
1T1R Multilevel

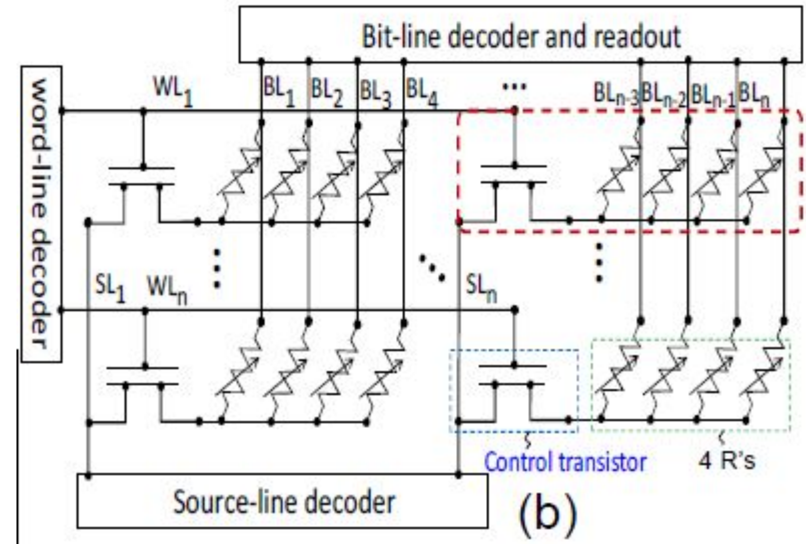


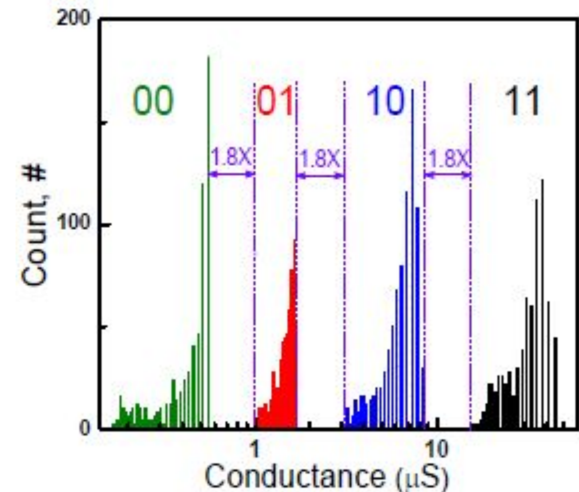
1T4R











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Summary

- Memory performance is critical to overall system performance
- On-chip SRAM very common today
  - 6T SRAM cells have become very compact
  - Complete memory architecture involves arrays + row/column decoders, sense amps, output drivers
- Nonvolatile memory has grown just as important.