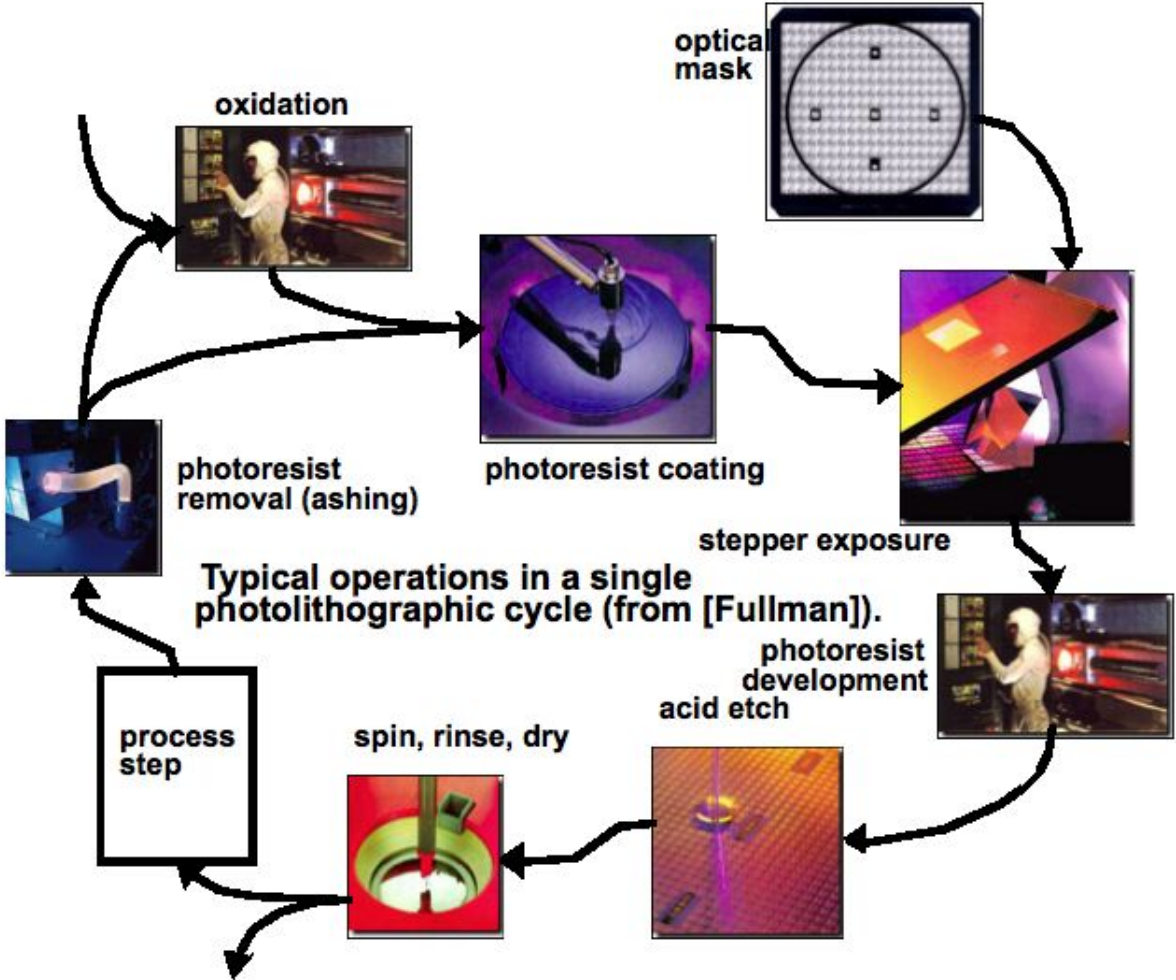


Design for Manufacturing

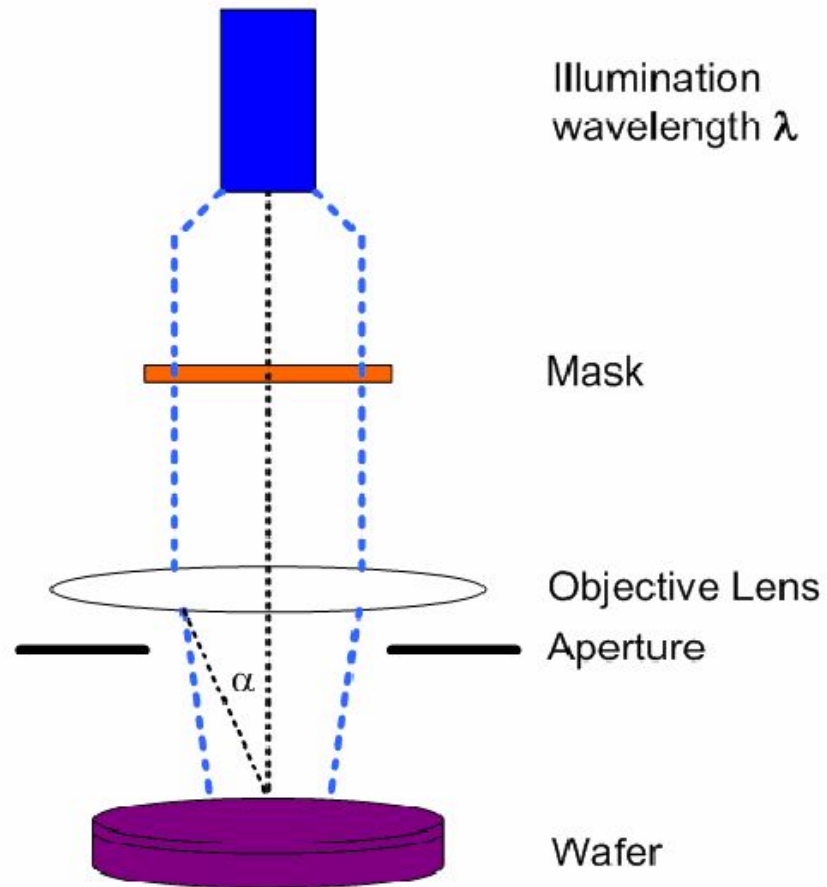
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Photo-Lithographic Process



Lithography systems



Lithography Primer: Basics

- The famous Raleigh Equation:

$$Resolution = k_1 \frac{\lambda}{NA}$$

λ : Wavelength of the exposure system

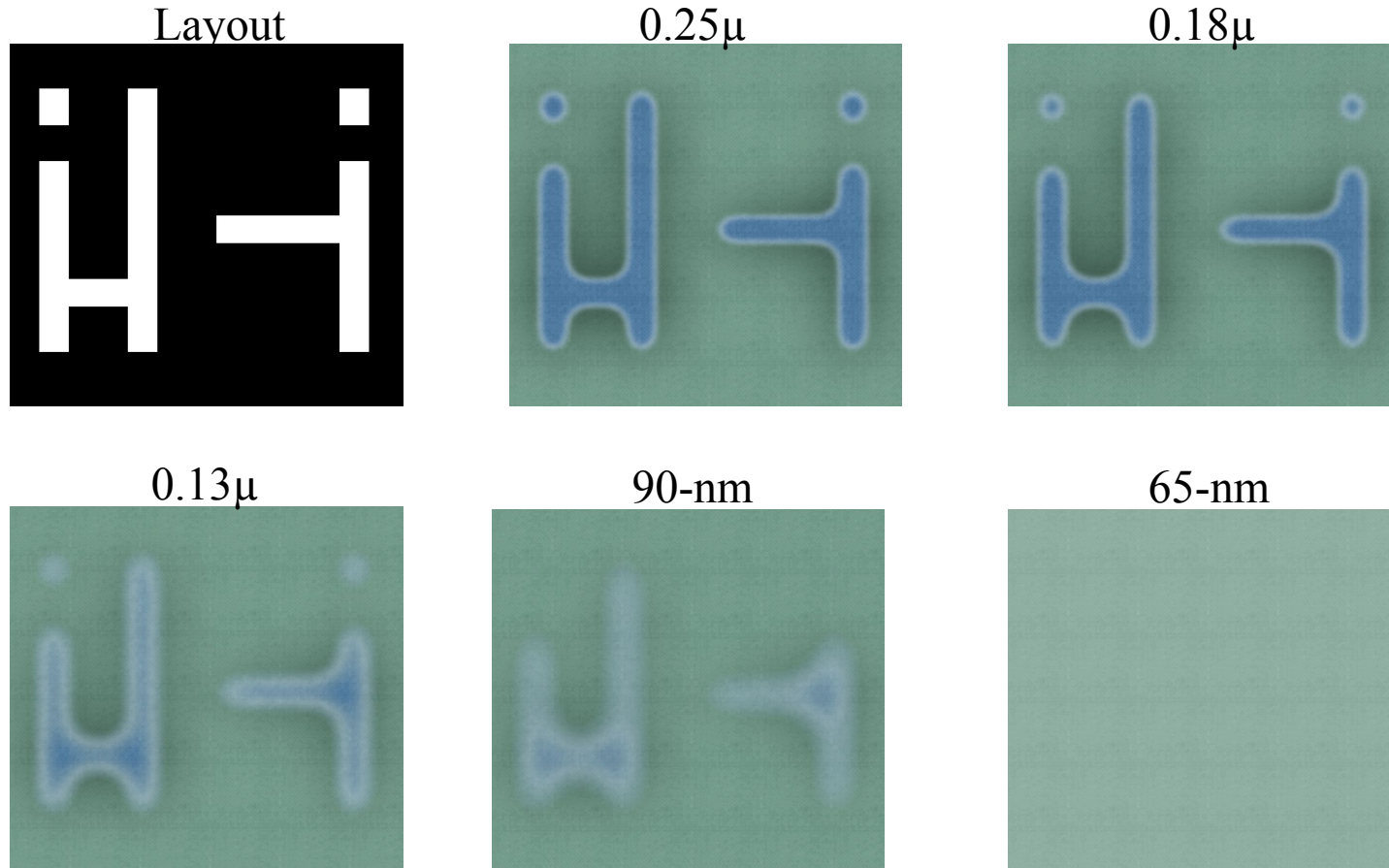
NA: Numerical Aperture (sine of the capture angle of the lens, and is a measure of the size of the lens system)

k_1 : process dependent adjustment factor

- Exposure = the amount of light or other radiant energy received per unit area of sensitized material.
- Depth of Focus (DOF) = a deviation from a defined reference plane wherein the required resolution for photolithography is still achievable.
- Process Window = Exposure Latitude vs. DOF plot for given CD tolerance



Mask versus Printing



Figures courtesy Synopsys Inc.

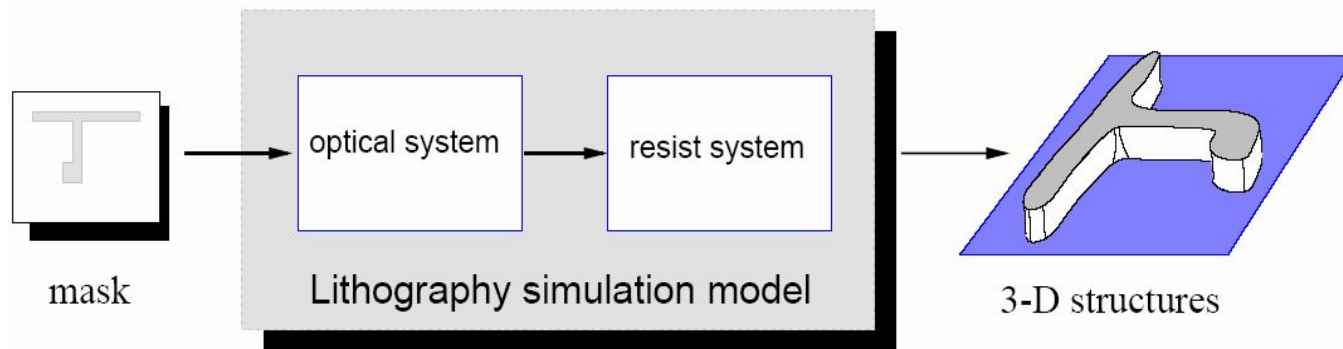
Lithography Model

To guide lithography aware physical design, *fast yet high-fidelity* lithography modeling/metrics are essential

Two key stages in litho-model (in a simplified view)

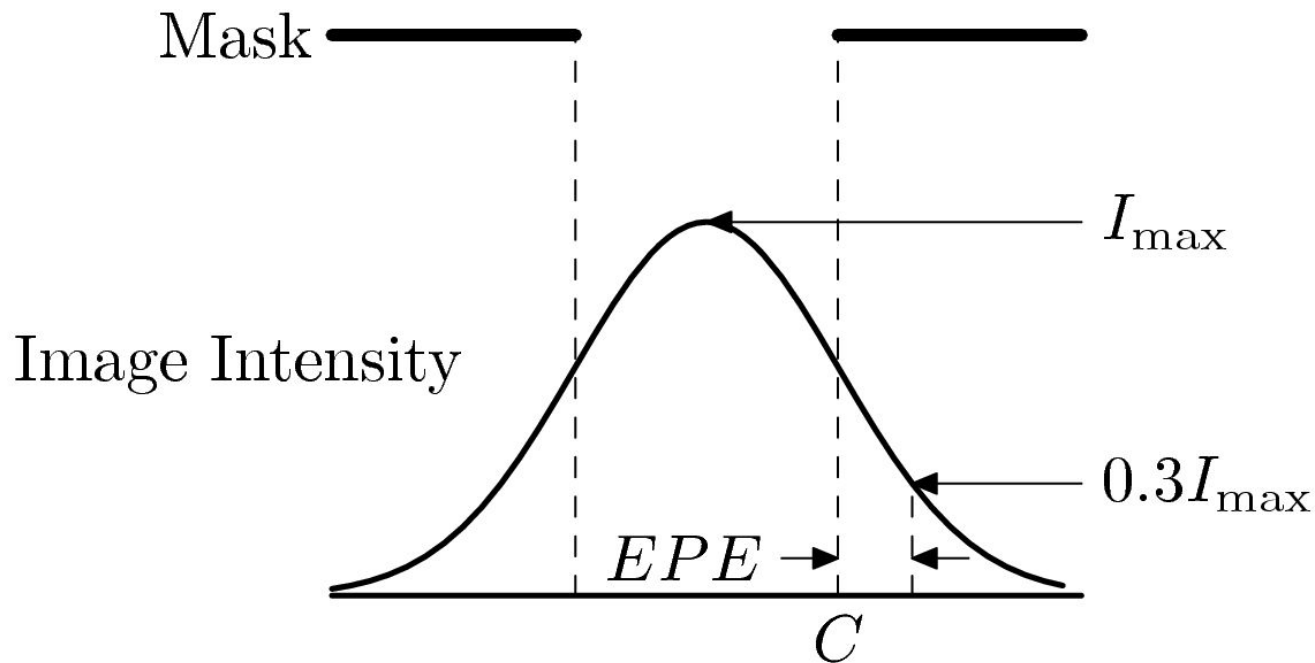
Optical system: will generate aerial image from mask

Resist system: photoresist and patterning inside the wafer



Simple Threshold Resist Model

- From the aerial image => printed image (resist model)
- Example: simple threshold model (e.g., $0.3I_{\max}$) to decide where to etch based on image intensity distribution

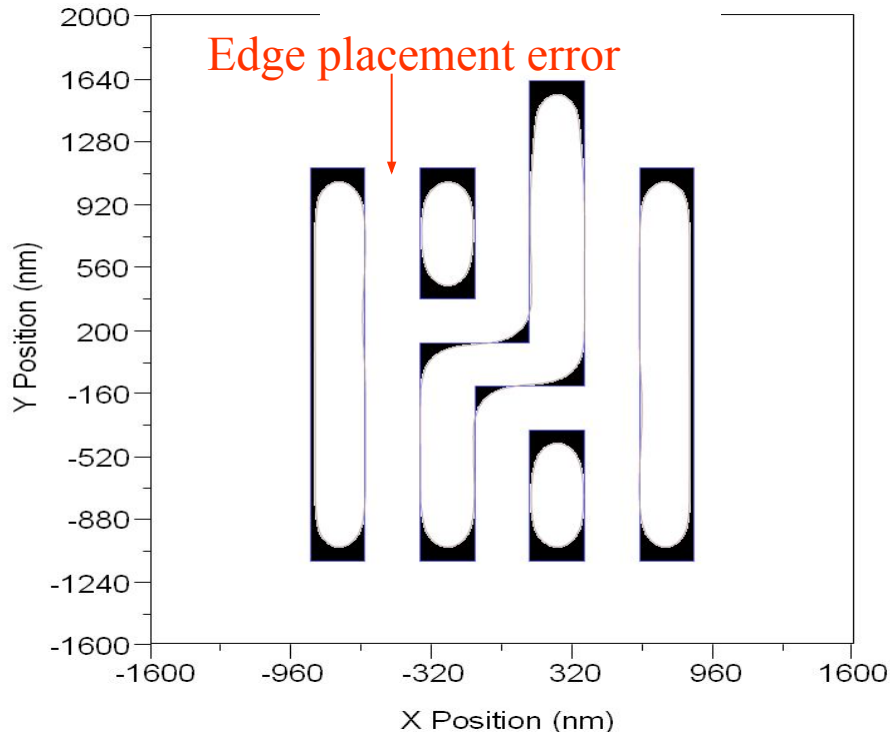


Edge Placement Error Map

A concept similar to congestion or thermal **hotspot** map

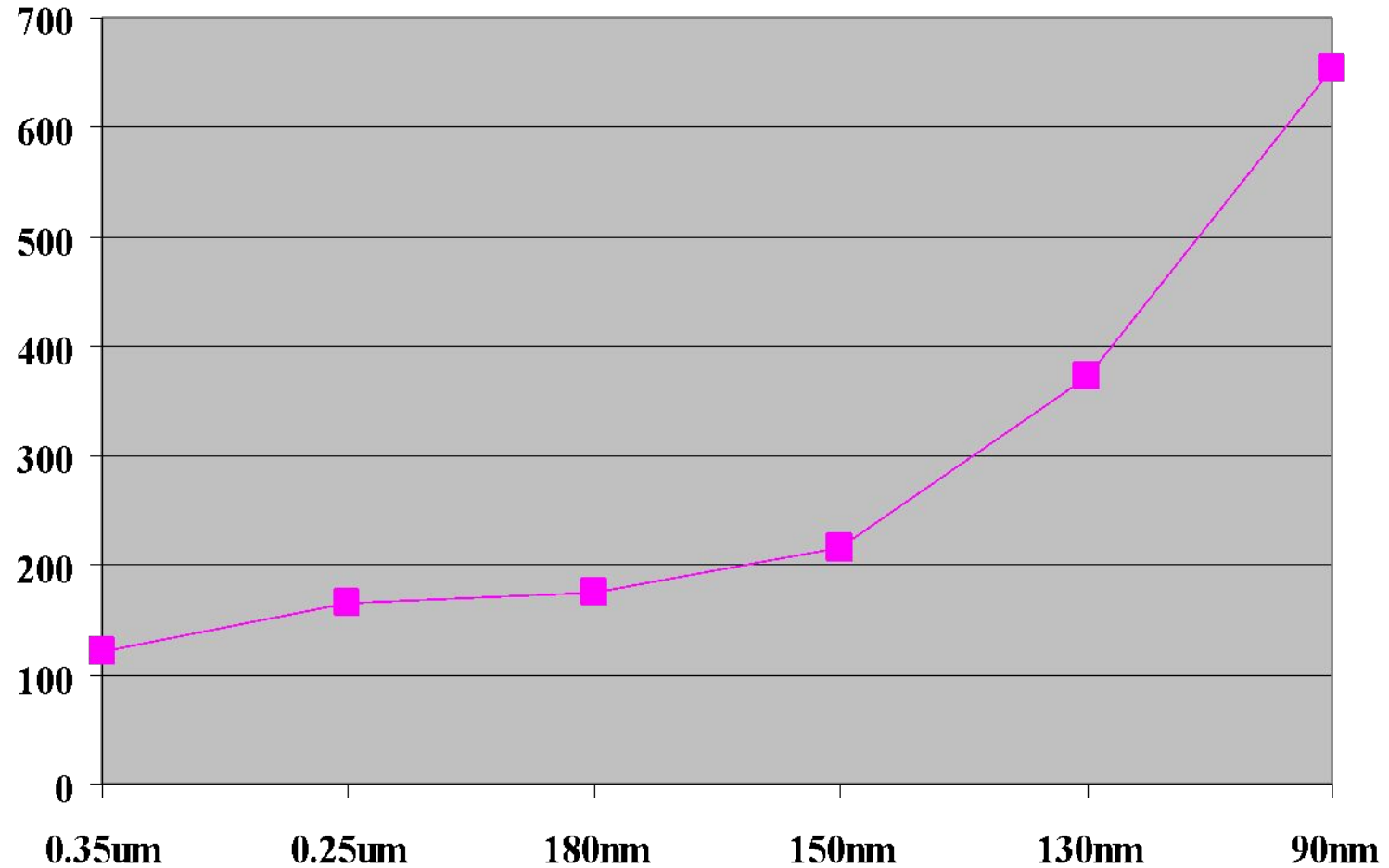
Measurement of RET **effort**

Work seamlessly with existing CAD flow



- ◆ Generate EPE for each “control point” (points that may have large edge placement errors) in design
- ◆ Each EPE control point has a ranked list of neighboring wires that contribute to the EPE
- ◆ Normalized EPE density for an entire segment

Design Rules Explosion



RET Basics

The light interacting with the mask is a wave

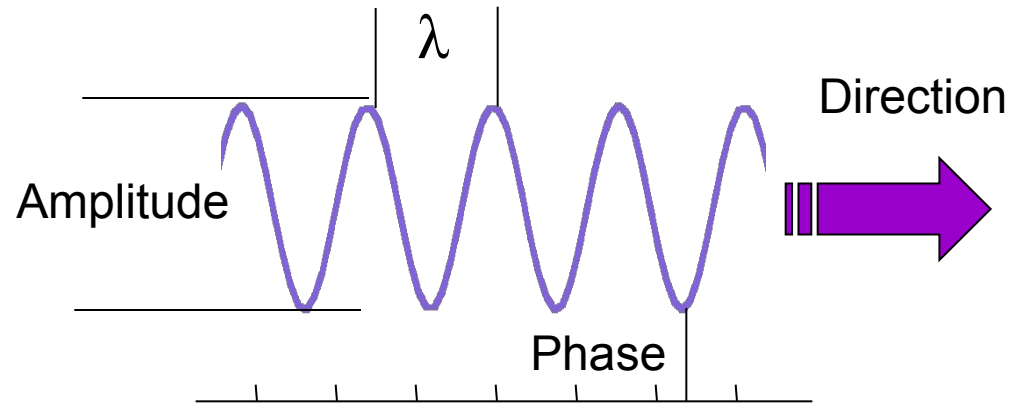
Any wave has certain fundamental properties

Wavelength (λ)

Direction

Amplitude

Phase



RET is wavefront engineering
to enhance lithography
by controlling these properties

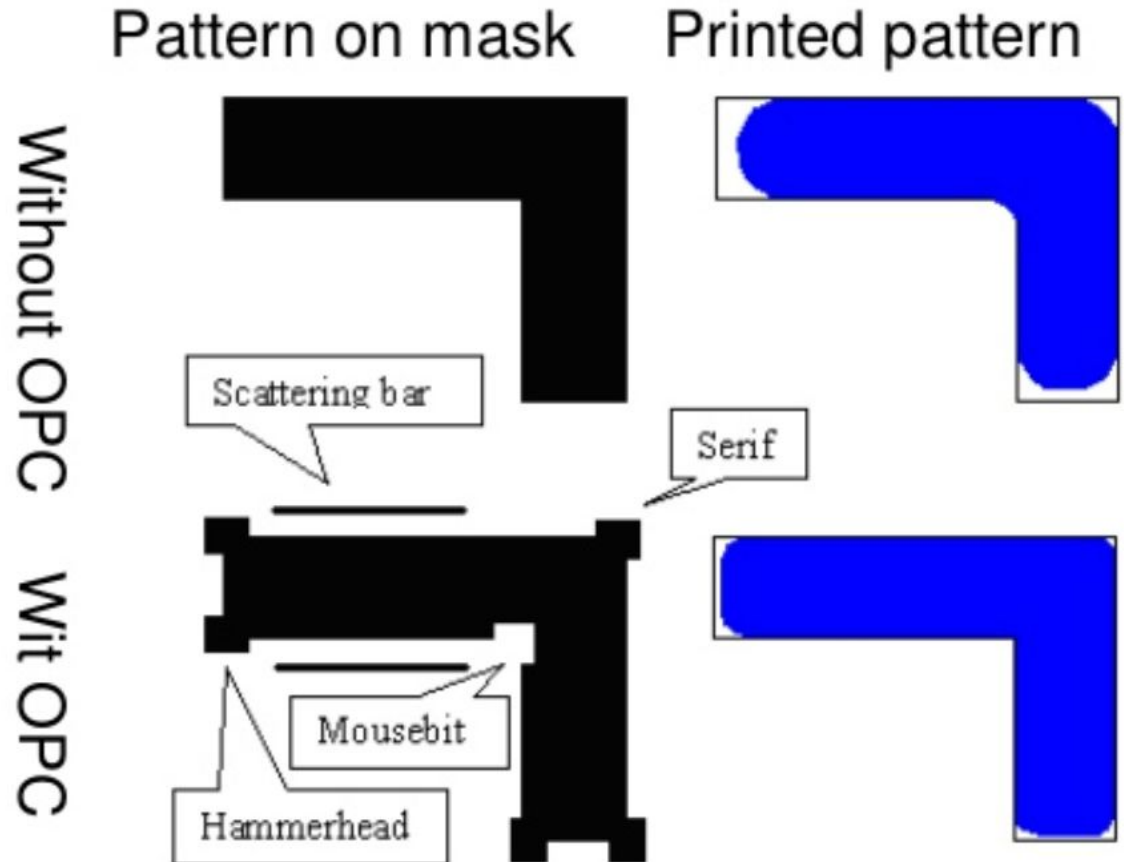
Courtesy F. Schellenberg, Mentor Graphics Corp.

Amplitude: OPC

Optical Proximity Correction (OPC) modifies layout to compensate for process distortions

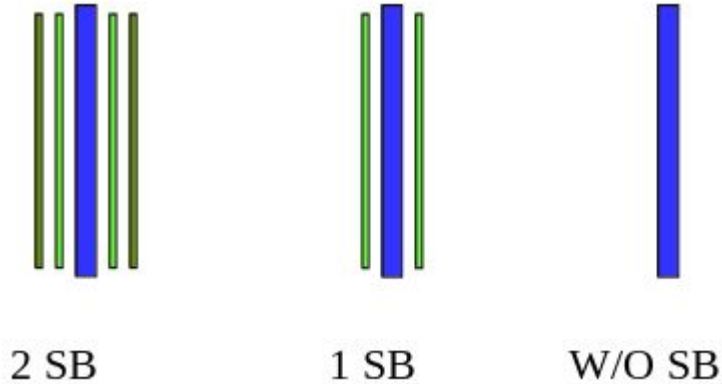
Add non-electrical structures to layout to control diffraction of light

Rule-based or model-based

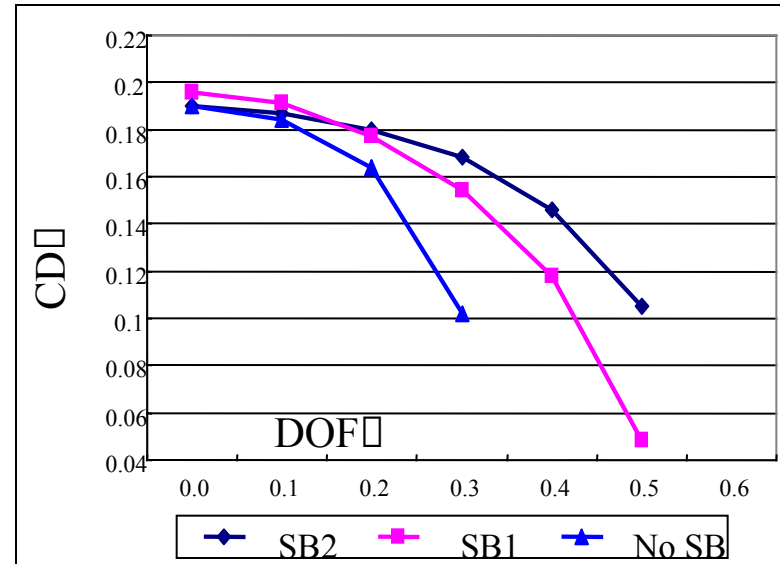


Assist Features and Variation

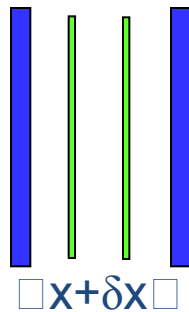
SB = Scattering Bar \equiv SRAF



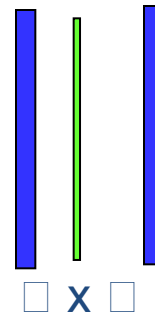
SRAFs are dummy geometries
Improve process window overlap for dense and isolated features
Not supposed to be printed
Unavoidable for 90nm poly



Layout Composability for SRAFs



Better than



Feature spacings are restricted to a small OR FIXED set

Two components

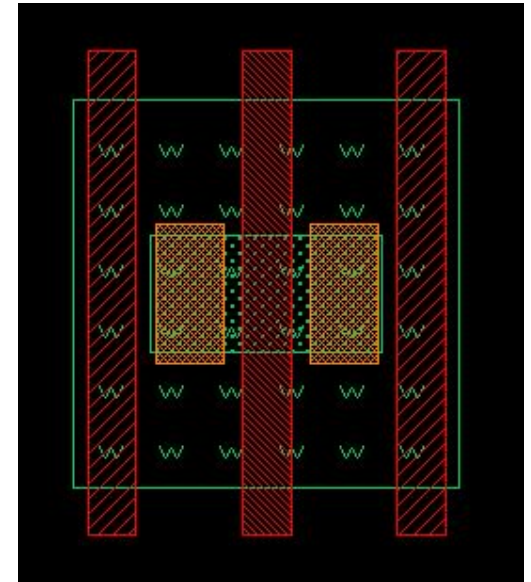
- Assist-correct library layouts □ Inter-device spacing within a standard cells □ Intelligent library design
- Assist-correct placement □ space between cells needs to be adjusted □ Intelligent whitespace management



Dual Patterning

It has gotten so bad, that some critical layers (e.g. metal1 and poly) are split into two separate masks.

No adjacent shapes are on the same mask to prevent diffraction problems.



Phase: PSM

Phase Shifting Masks (PSM) etch topography into mask

Creates interference fringes on the wafer

□ Interference effects boost contrast □ Phase

Masks can make extremely small gates

conventional mask



glass

Chrome

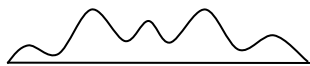
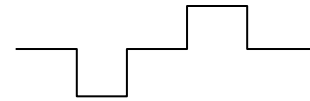
phase shifting mask



Phase shifter



Electric field at mask

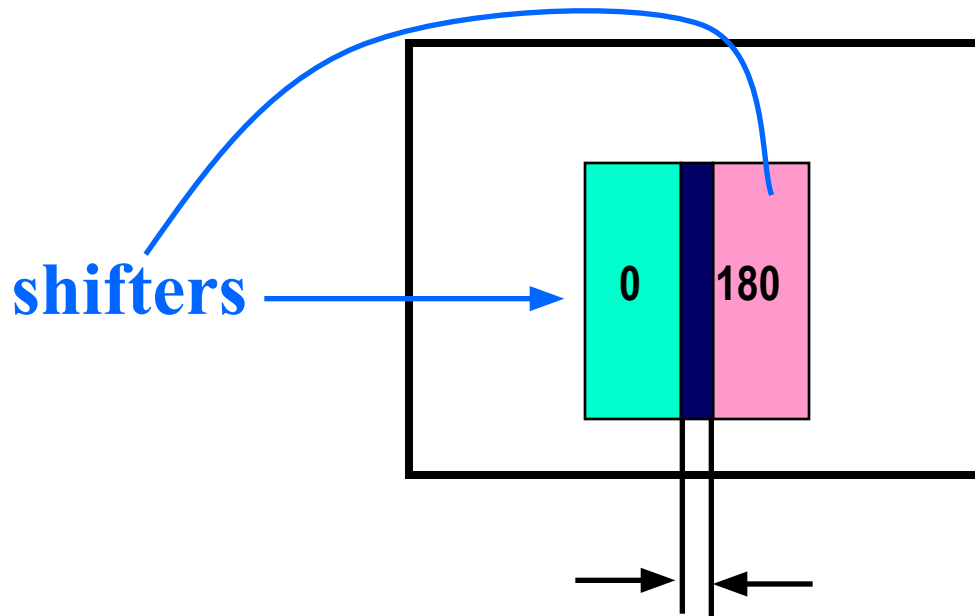


Intensity at wafer



The Phase Assignment Problem

Assign 0, 180 phase regions such that critical features with width $< B$ are induced by adjacent phase regions with opposite phases

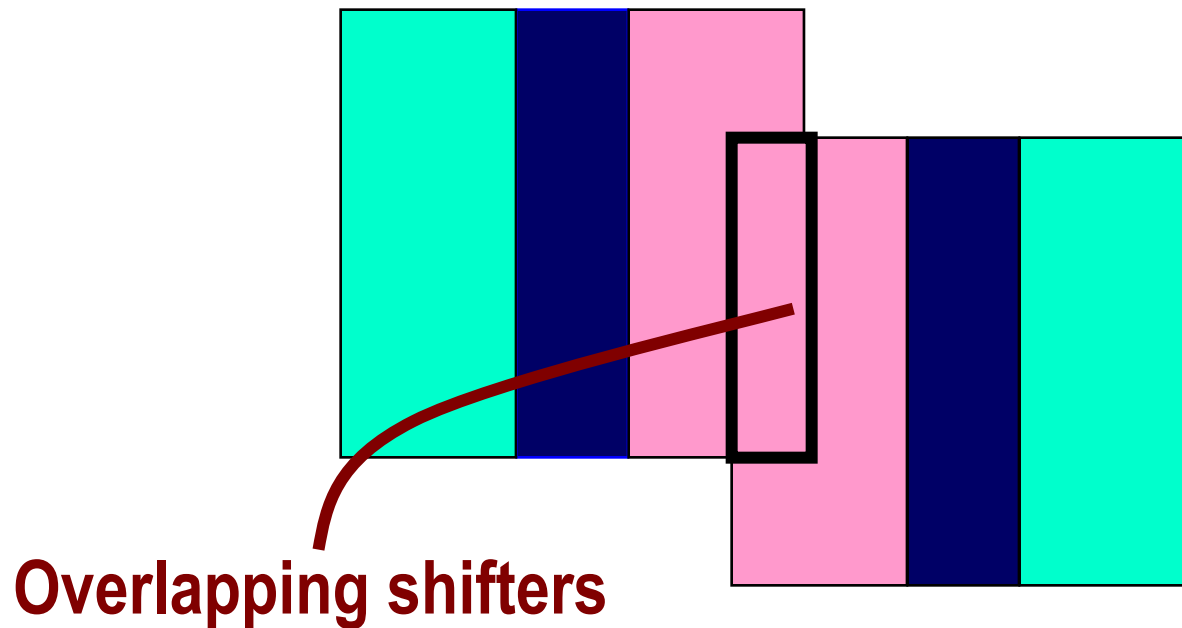


Phase Assignment for Bright-Field PSM

PROPER Phase Assignment:

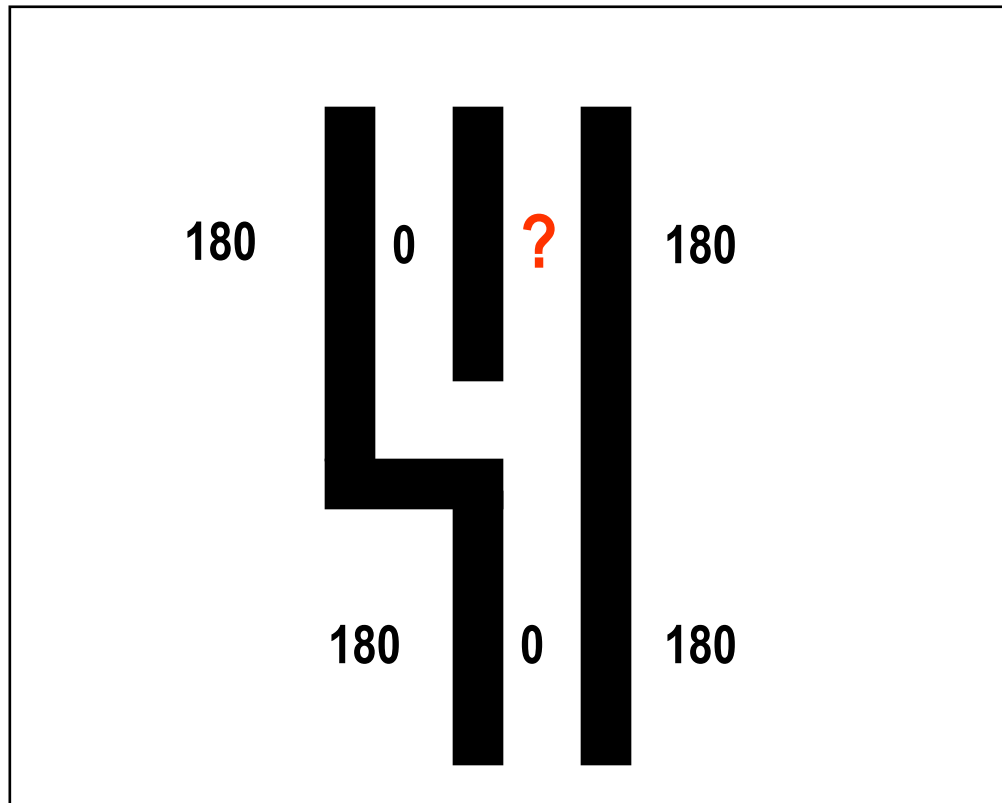
Opposite phases for opposite shifters

Same phase for overlapping shifters

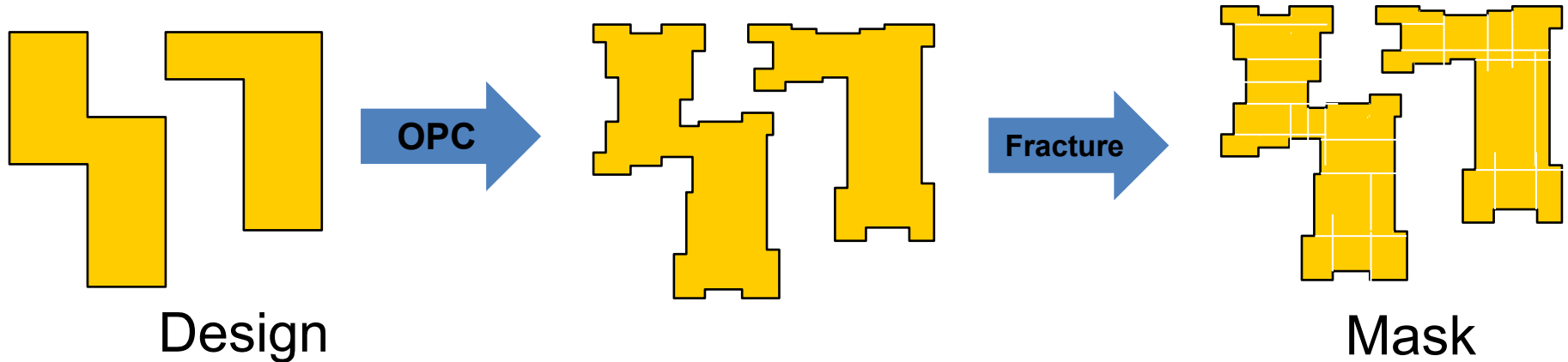


Key: Global 2-Colorability

Odd cycle of “phase implications” → layout cannot be manufactured
layout verification becomes a global, not local, issue



Mask Costs



Mask Cost \propto Data Volume

- OPC, PSM, Fill increased feature complexity
- increased mask cost

Figure courtesy Synopsys Inc.