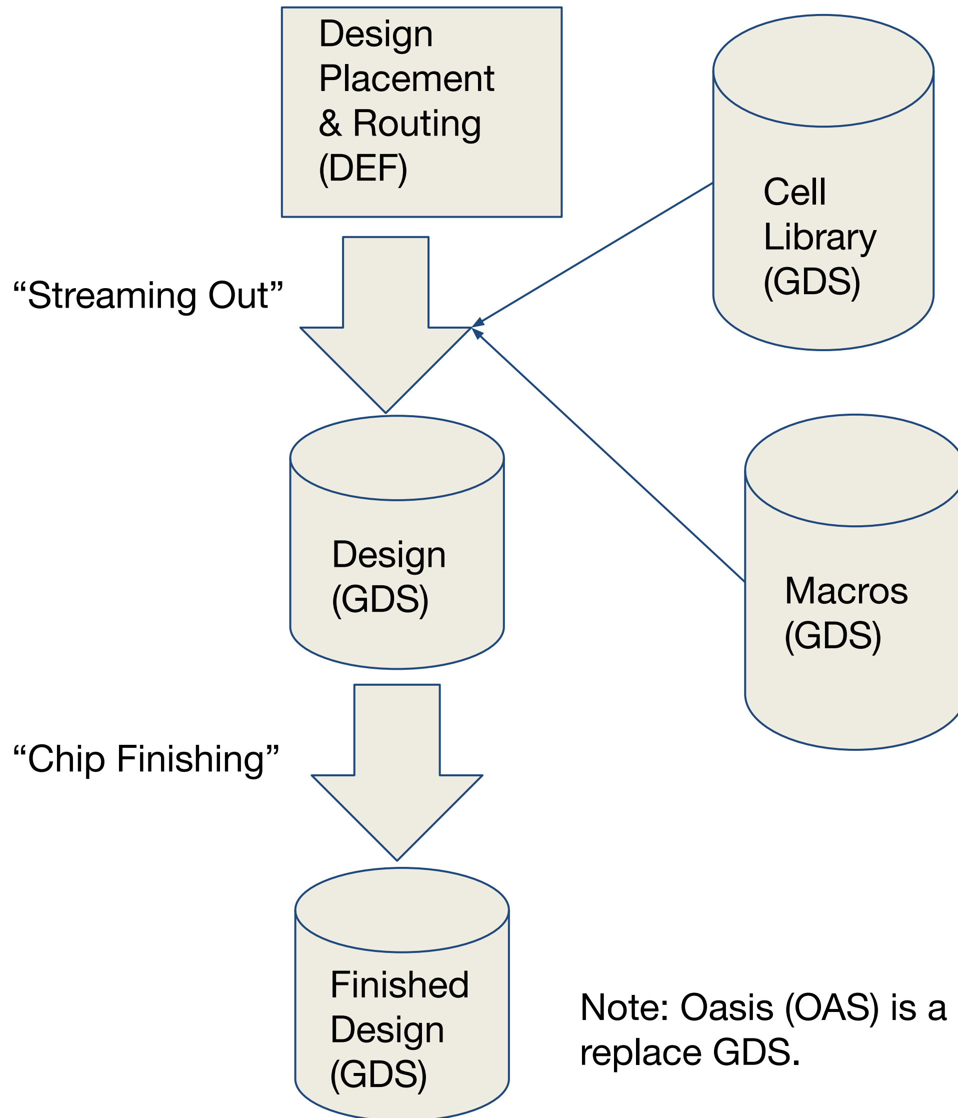
Lecture 16: Chip Finishing

Matthew Guthaus
Professor
UCSC, Computer Science & Engineering
http://vlsida.soe.ucsc.edu
mrg@ucsc.edu

GDS Generation



Note: Oasis (OAS) is a newer format that is slowly starting to replace GDS.

Today's Lecture

- Metal Density
- Antenna Checks
- Latch-Up
- IR Drop/Decoupling Capacitance
- Electromigration

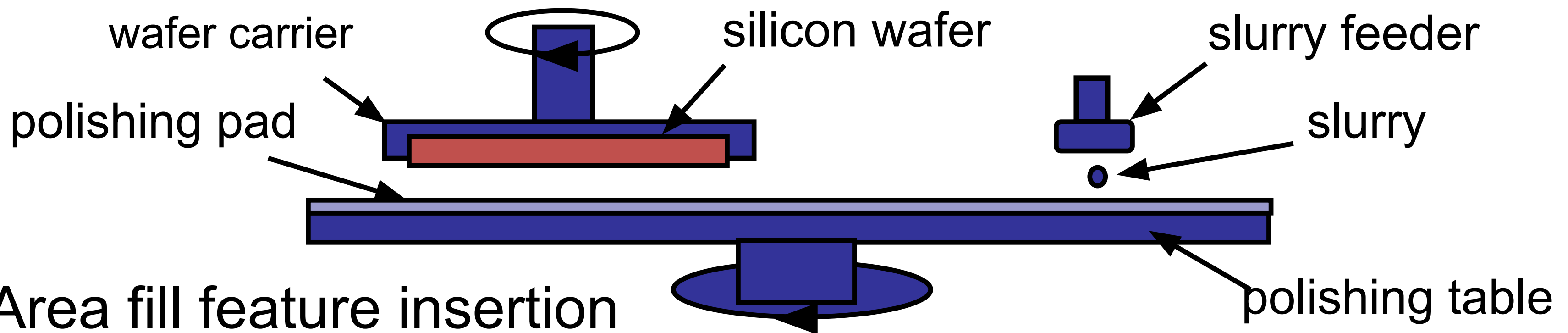
Today's Lecture

- Metal Density
- Antenna Checks
- Latch-Up
- IR Drop/Decoupling Capacitance
- Electromigration

CMP & Area Fill

Chemical-Mechanical Planarization (CMP)

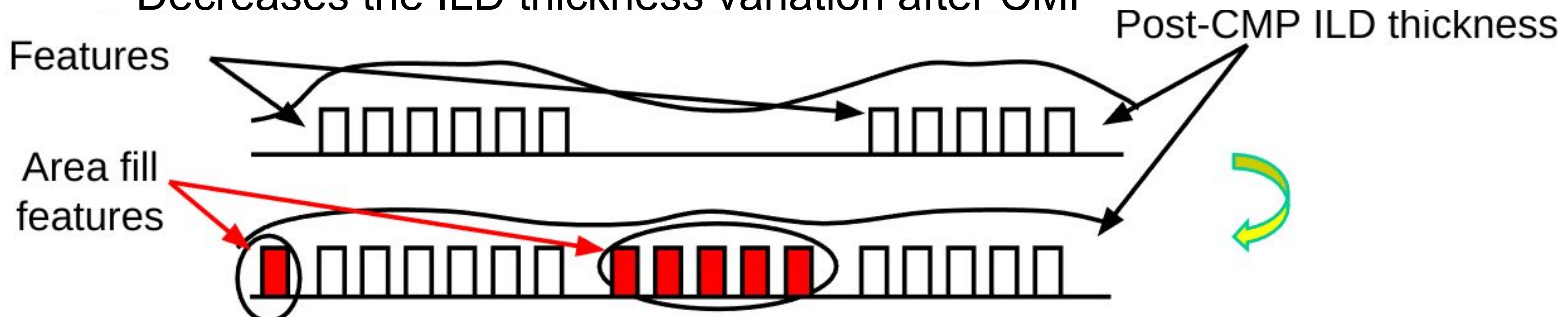
Polishing pad wear, slurry composition, pad elasticity make this a very difficult process step



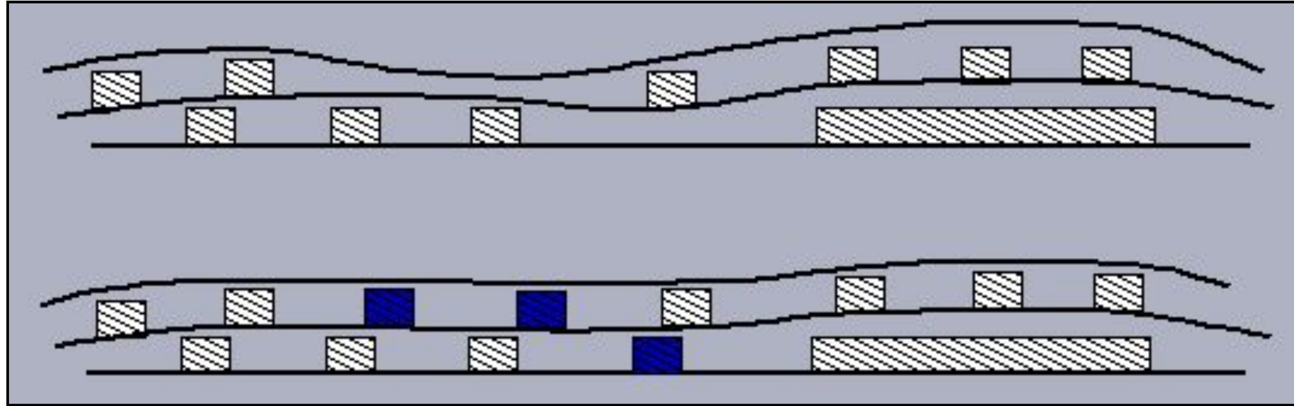
Area fill feature insertion

Decreases local density variation

Decreases the ILD thickness variation after CMP

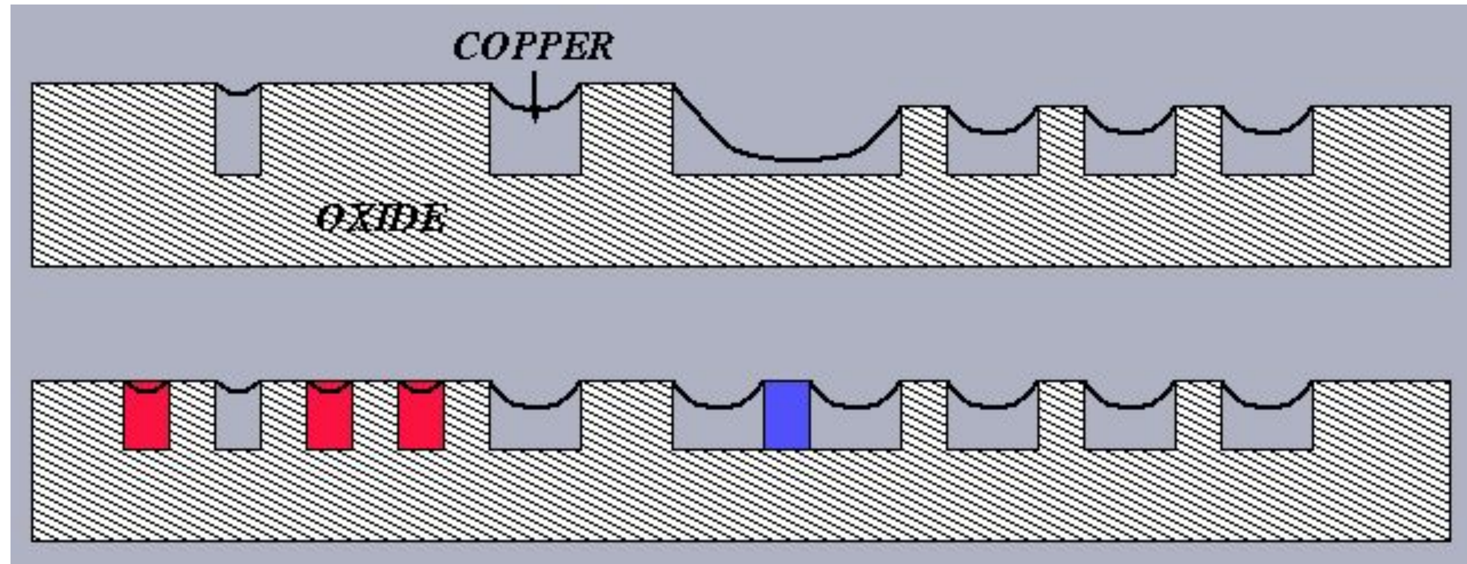


Tiling for ILD (Al Metallurgy)



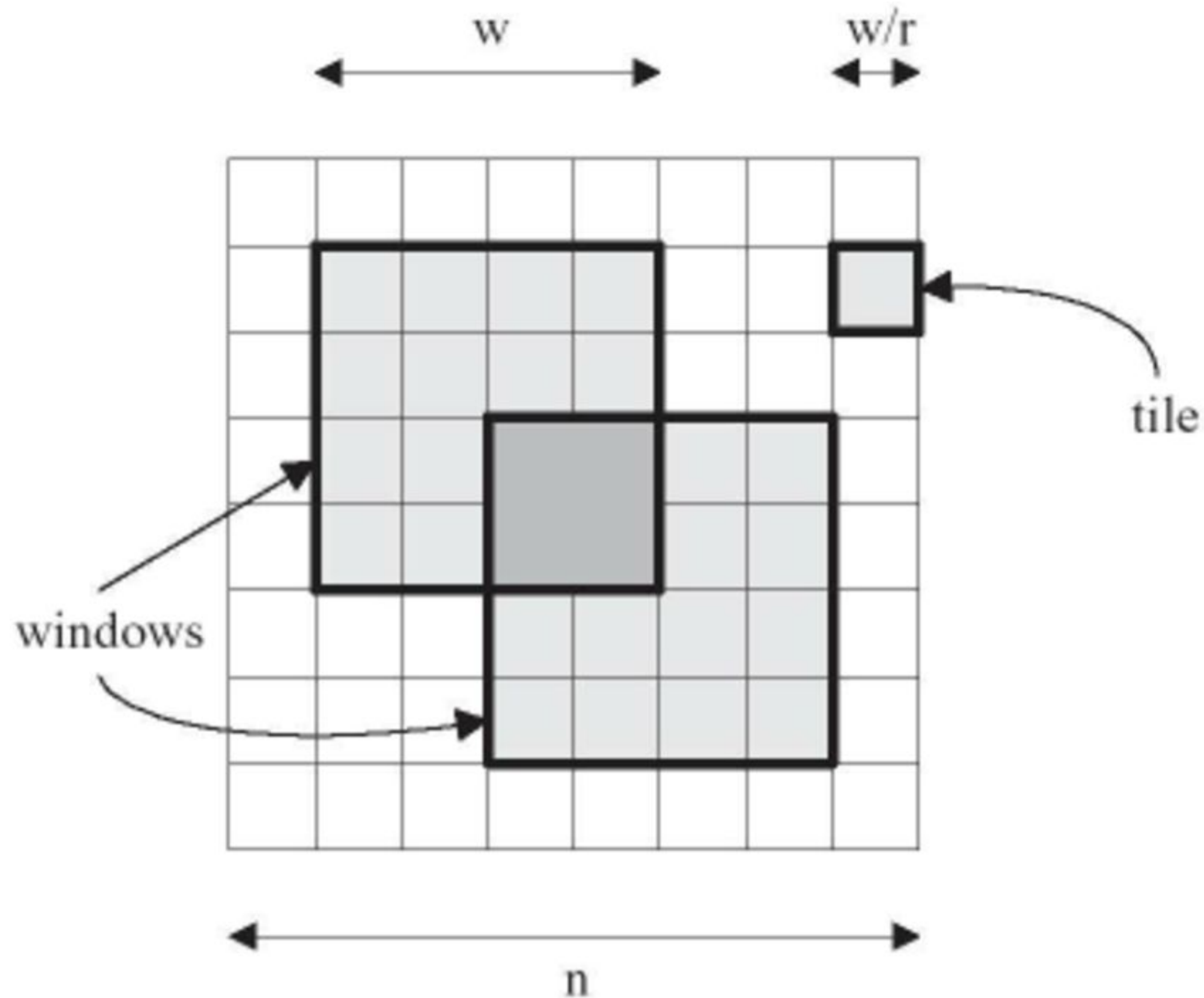
- Single Material Polish: A Linear Model is Sufficient
- Cumulative Effect Also Captured by Linear Models

Tiling for Copper CMP



- Tiling and Slotting: Both Oxide Erosion and Copper Dishing need to be controlled.
- Three Polish Stages: Overburden copper removal, Barrier removal, and Oxide over polish.
- Planarity Solution - Research Topic

Density Computation



Density Control Objectives

Objective for Manufacture = Min-Var [Kahng et al., TCAD'02]

minimize **window** density variation

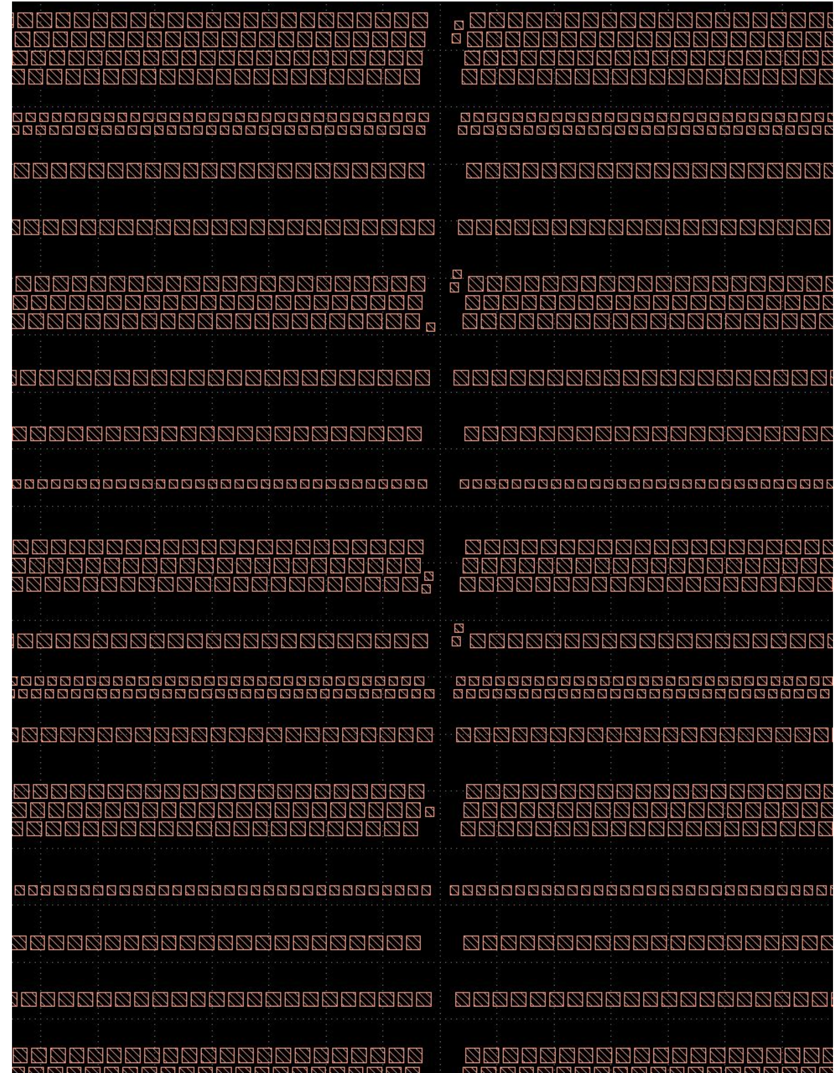
subject to upper bound on window density

Objective for Design = Min-Fill [Wong et al, DAC'00]

minimize **total amount** of added fill

subject to UB on window density variation

M5 Fill Example



Complex Fill Example

Issues with Fill

- Adds coupling capacitance
  - Now need to extract + signoff again
  - Timing-driven fill insertion

Tiling and its Impact on PD

The Tiling Problem:

Given a layout and a CMP model, determine the location and amount of dummy features needed to achieve a planarity target, and then modify the layout accordingly.

- **Planarity Target <-> PD Resolution Requirement**
- **Application: ILD, STI, and Copper Tiling**
- **Tiling Effectively Modifies the Physical Design**
  - **Reticle/Die Array on Wafer Level Design**
- **Mask Inspection Issues (die to die matching)**

Today's Lecture

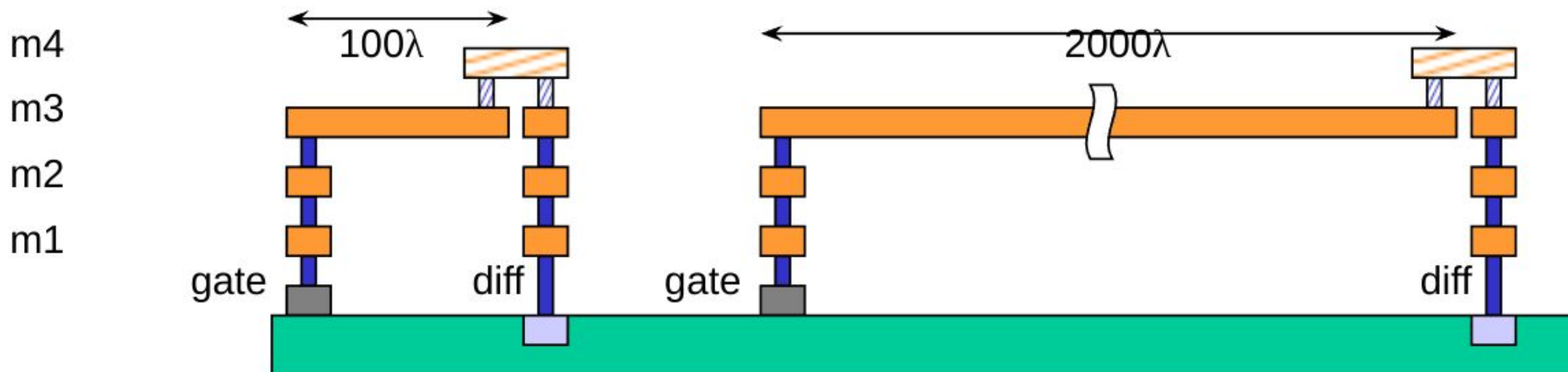
- Metal Density
- Antenna Checks
- Latch-Up
- IR Drop/Decoupling Capacitance
- Electromigration

Antenna rules (an ERC)

- Charging in semiconductor processing
  - Many process steps use plasmas, charged particles
  - Charge collects on conducting poly, metal surfaces
  - Large amounts of charge on poly can create huge E-fields across the thin gate oxide and lead to breakdown
  - Amount of charge collected is proportional to area of conductors
- Important ratio: antenna ratio defined as:
  - $(A_{poly} + A_{M1} + \ldots) / A_{gate_ox}$
  - A_{Mx} = metal x area electrically connected to node
    - This is very conservative as higher levels of metal can alleviate the problem
  - If a diode is attached along the line, antenna rules are relaxed
    - Provides a low impedance path for large amounts of charge to be removed from the conductor

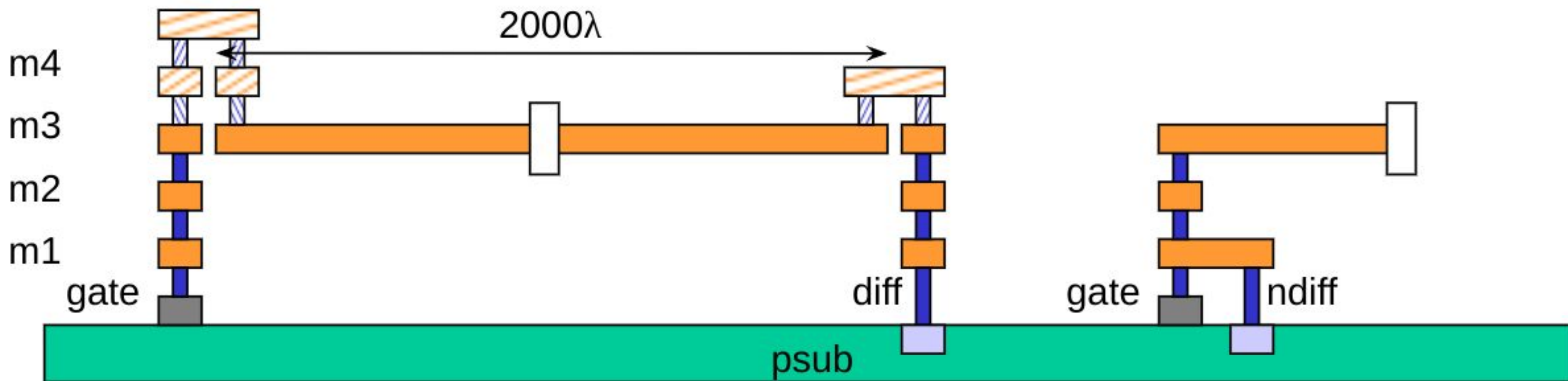
Antenna rules (an ERC)

- Reactive ion etch charges up metal lines
  - Charge can accumulate and zap a gate oxide
  - If a gate sees a **long** metal before a diffusion does



Antenna rules (an ERC)

- Two solutions: bridging and node diodes
  - Bridging attaches a higher layer intermediary
  - Diode is a piece of diffusion to leak away charge



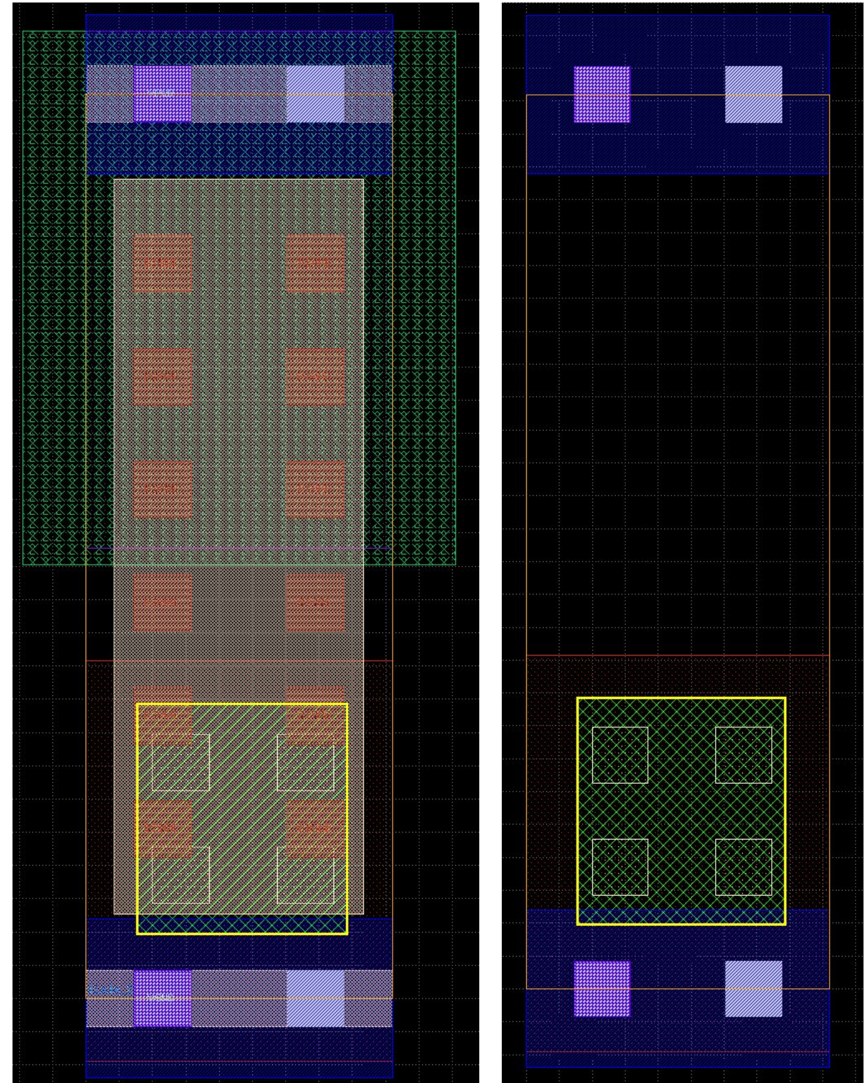
Bridging keeps gate away from long metals until they drain through the diffusion

Node diodes are inactive during chip operation (reverse-biased p/n); let charge leak away harmlessly

Sky130 Diode Cell

Yellow “diode” layer

diff + nsdm + substrate

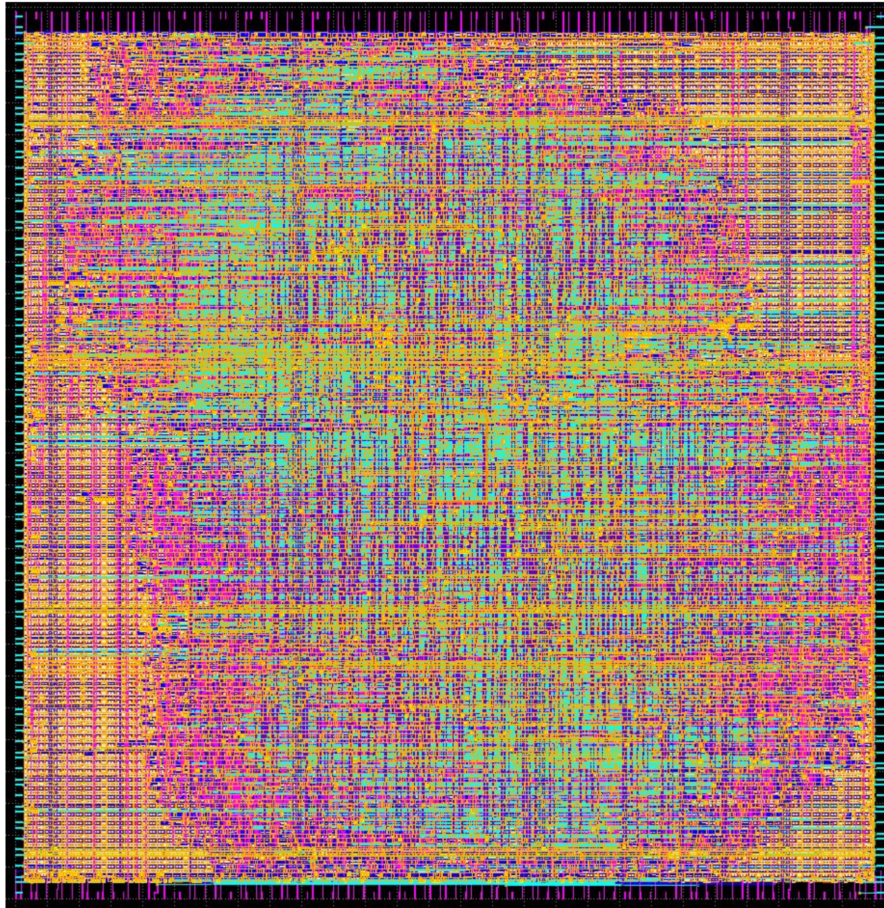


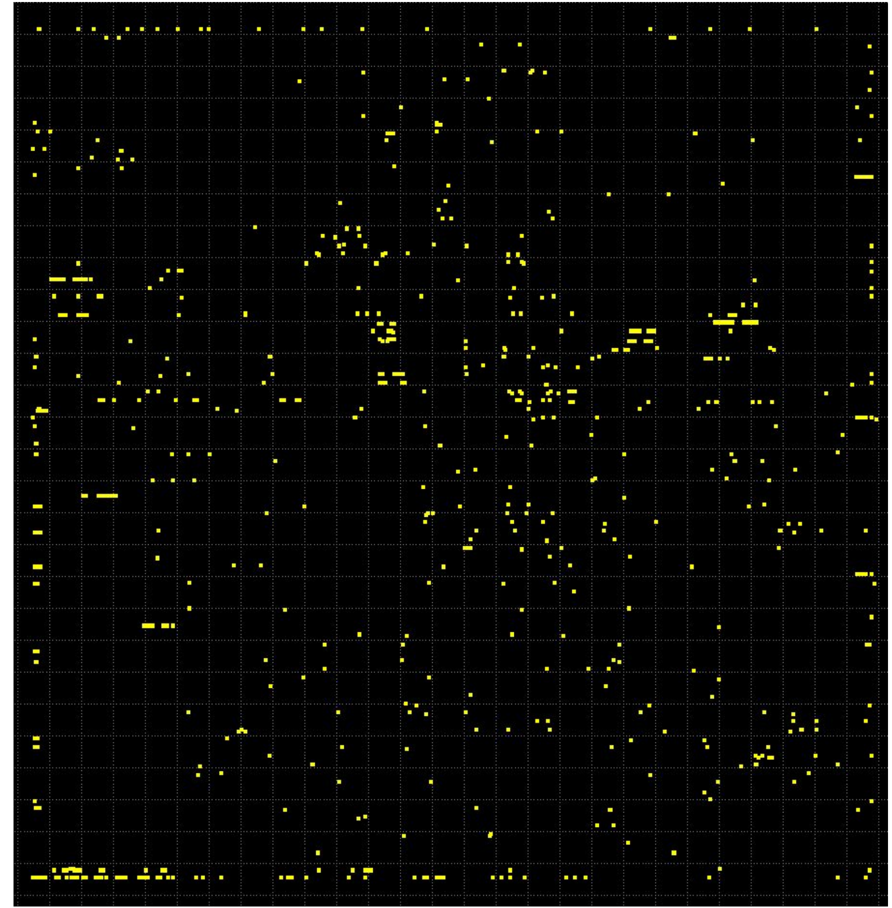
OpenLane Diode Options

DIODE_INSERTION_STRATEGY Variable

1. No diode insertion is done.
2. A diode is inserted for each PIN and connected to it.
3. **A fake diode is inserted for each PIN and connected to it, then after an antenna check is run and the fake diodes are replaced with real ones if the pin is violated.**
4. Rely on OpenROAD:FastRoute antenna avoidance flow to insert the diodes during global routing by using the Antenna Rule Checker and fixing violations. You can execute this iteratively by setting GRT_MAX_DIODE_INS_ITERS, it is capable to detect any divergence, so, you will probably end up with the lowest # of Antenna violations possible.
5. A smarter version of strategy 1 that attempts to reduce the number of inserted diodes and places a diode at each design pin.
6. A variant of 2 utilizing the script used in strategy 4.

How many diodes are inserted?





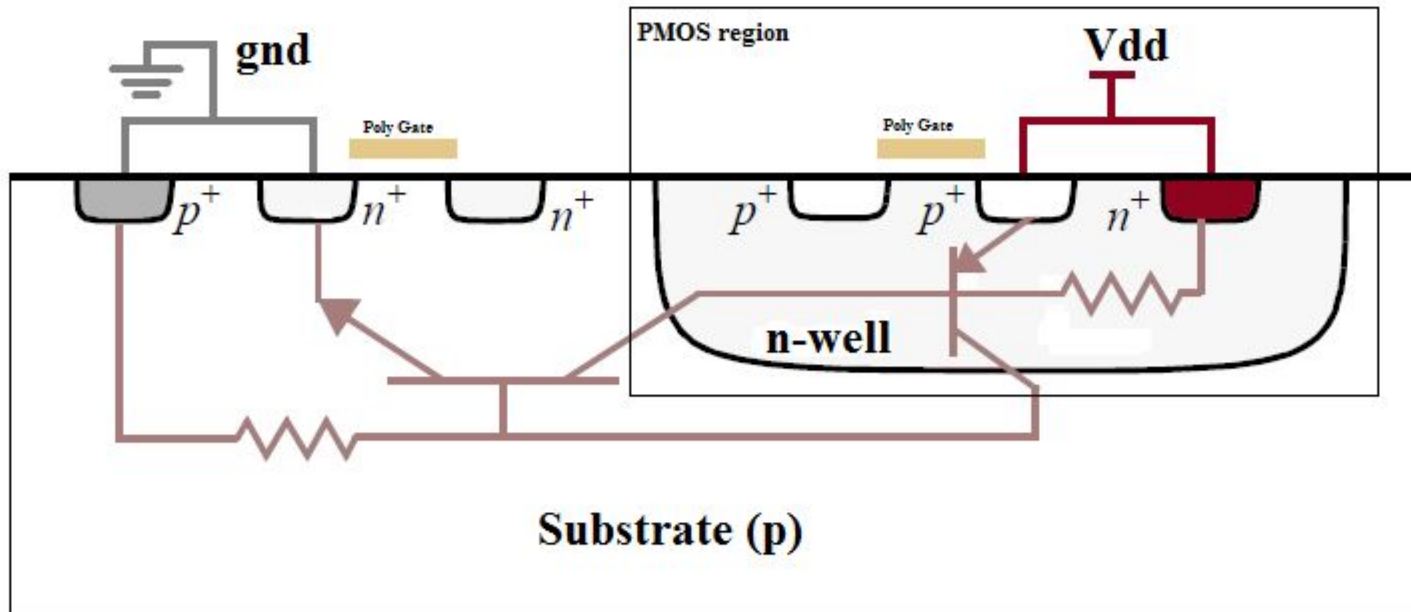
Today's Lecture

- Metal Density
- Antenna Checks
- Latch-Up
- IR Drop/Decoupling Capacitance
- Electromigration

Latch Up (an ERC)

- Causes shorting of VDD & VSS lines
- Result:
  - Destroys chip or
  - Causes system failure – must power down to fix
- Control with process innovations & circuit design

Parasitic Transistor Location



Solutions to Latchup

- Solutions:
  - Reduce R values
  - Reduce bipolar transistor gains
- Prevention:
  - Latchup-resistant CMOS processes
  - Layout techniques

V_{DD}

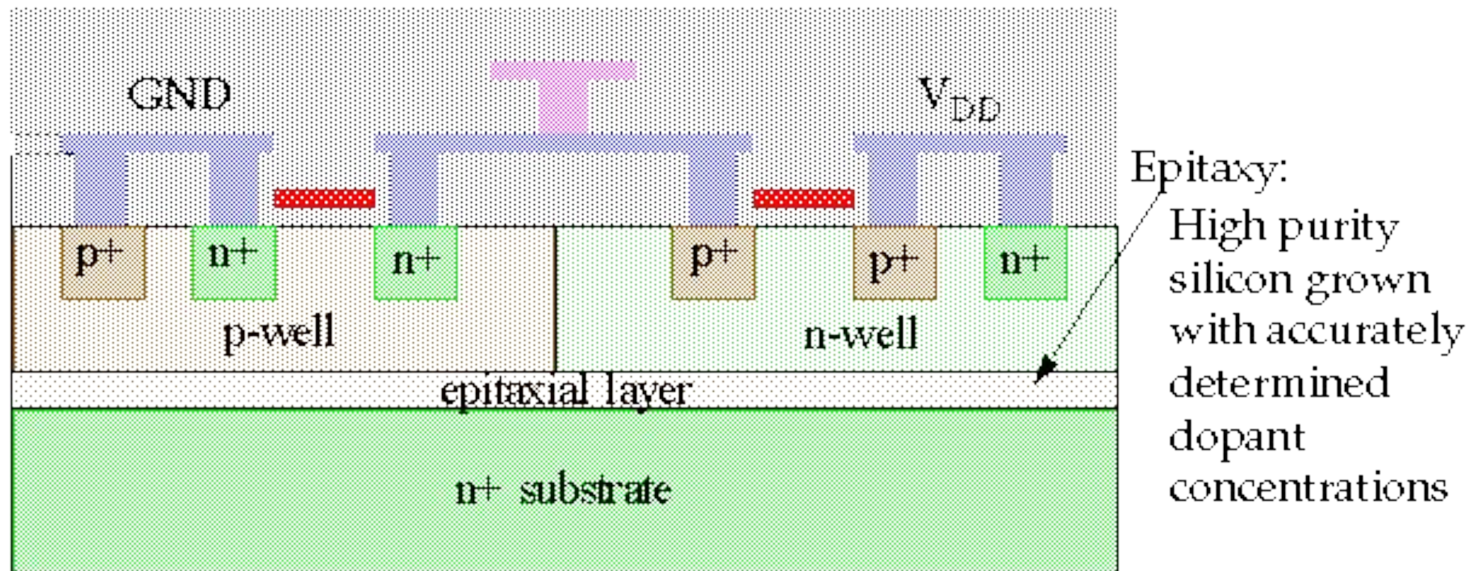
R(nwell)

p-n-p

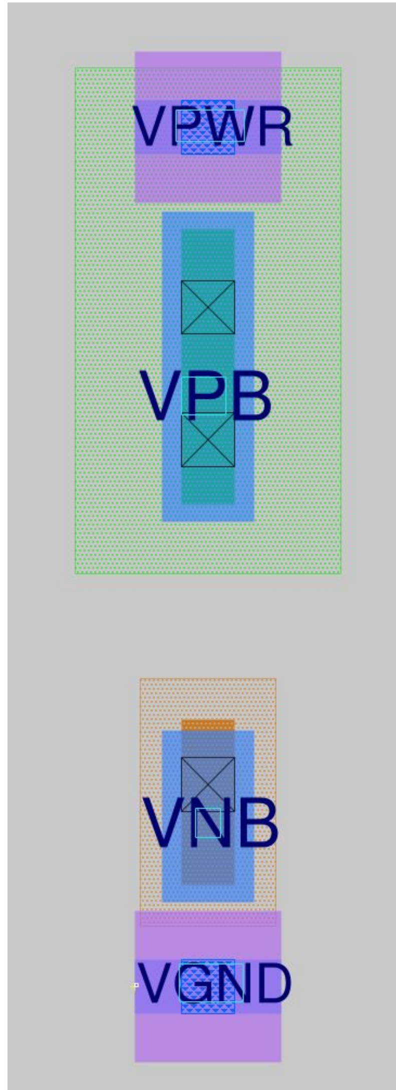
n-p-n

R(pwell)

Well Contacts



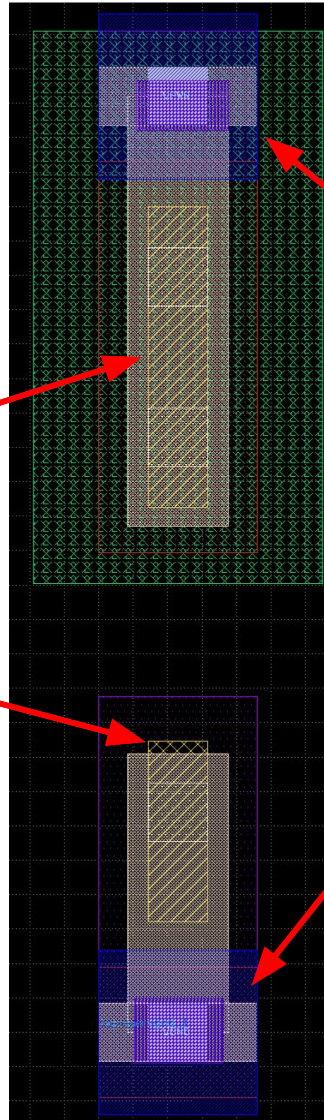
Sky130 “tap” Cell



VGND
VNB
VPB
VPWR

GND
V_{DD}
p+
n+
n+
p+
p+
n+
p-well
n-well
epitaxial layer
n+ substrate

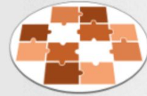
Sky130 Tap Cell



Connection to supplies

“tap” layer says make “diff” same as well type

Latch-Up Workshop



Latch-Up

Friday, March 31 to Sunday, April 2, 2023 in Santa Barbara, California, at University of California, Santa Barbara (UCSB)

© ChrisGoldNY CC BY 3.0

About

The FOSSi Foundation is proud to announce Latch-Up, a conference dedicated to free and open source silicon to be held over the weekend of **Friday, March 31 to Sunday, April 2, 2023** in Santa Barbara, California, USA. (Venue details)

Latch-Up is a weekend of presentations and networking for the open source digital design community, much like its European sister conference ORConf.

So save the date, register to attend, and we encourage you to submit a presentation or proposal if you have a project or idea on the topic to share!

Questions? Ping the organizers via @LatchUpConf or email.

Previous Latch-Ups: 2019 Portland · (Latch-Up 2020 was planned to take place in Cambridge, MA, but had to be cancelled.)

Submit a talk

We encourage anybody involved in the open source semiconductor engineering space to come along and share your work or experience. Presentations slots as short as 3 minute lightning-talks and up to 30 minute talks including Q and A are available.

So if you've designed, worked on or even just used open source IP cores and/or management systems, verification IP, build flows, SoCs, simulators, synthesis tools, FPGA and ASIC implementation tools, languages and DSLs, compilers, or anything related we'd love to have you join us to share your experience.

Presentations are submitted through the registration process and we will let you know if your presentation was accepted.

Sponsors

z e r |o|

Latch-Up is an excellent opportunity for sponsors to show their support for the open source silicon community. Interested? Read our sponsorship flyer to learn more

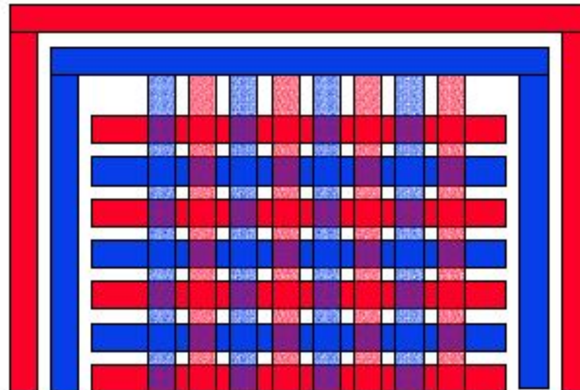
Get in touch to become a sponsor

Today's Lecture

- Metal Density
- Antenna Checks
- Latch-Up
- IR Drop/Decoupling Capacitance
- Electromigration

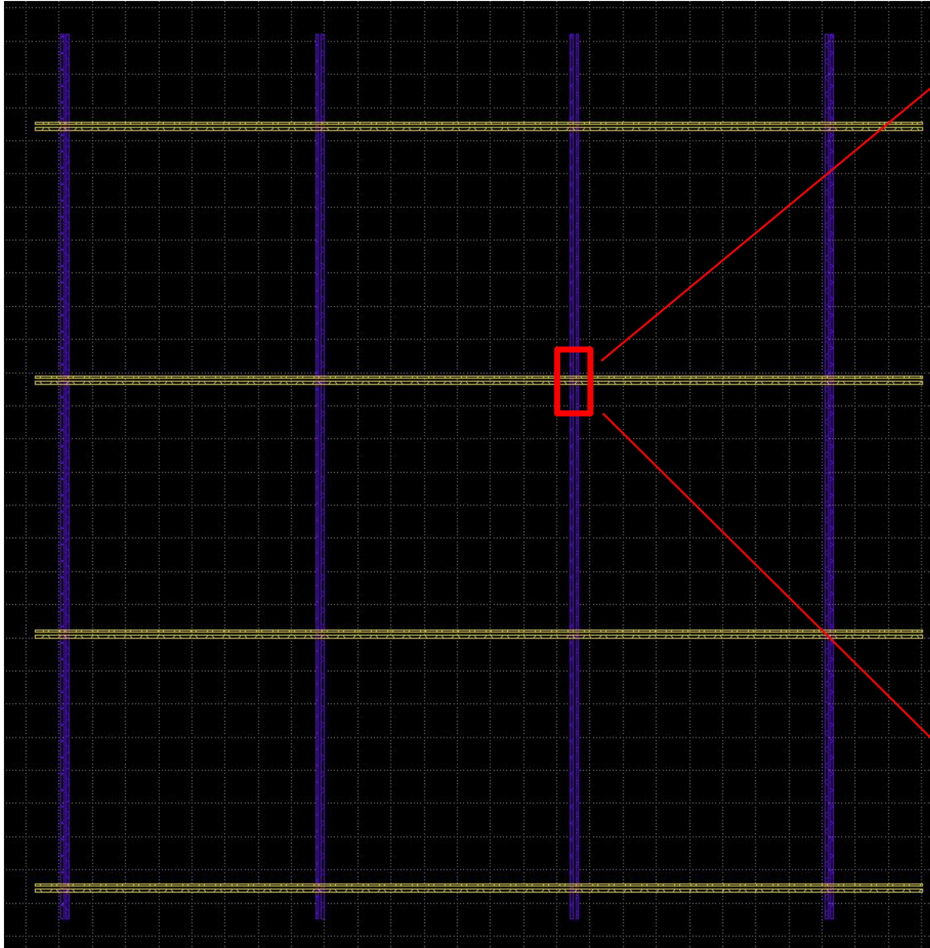
P/G Mesh (Grid Distribution)

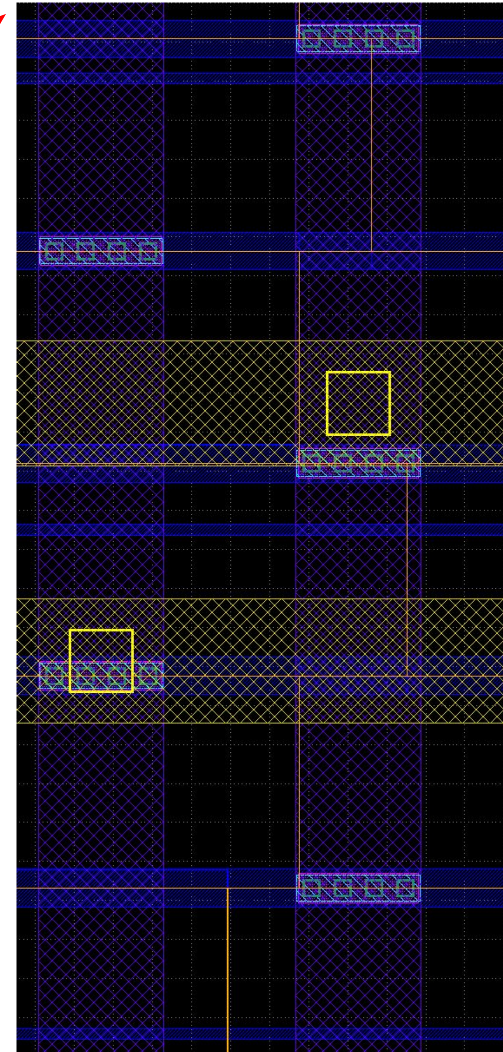
- Power/Ground mesh will allow multiple paths from P/G sources to destinations
  - Less series resistance
  - Hierarchical power and ground meshes from upper metal layers to lower metal layers
    - All the way to M1 or M2 (standard cells)
  - Connection of lower layer layout/cells to the grid is through vias



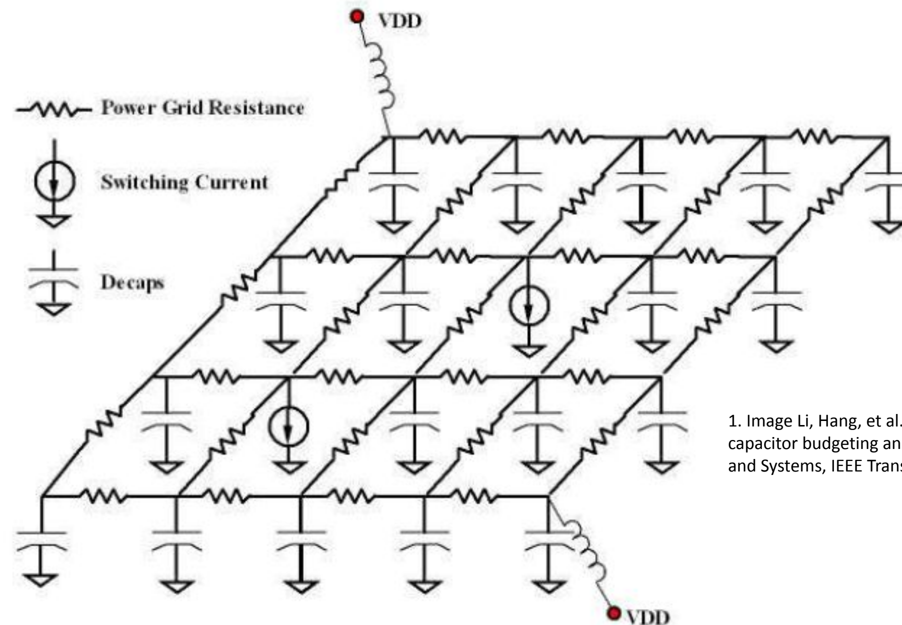
Sky130 Power Supply

M4 vertical, M5 horizontal





Power Supply Networks

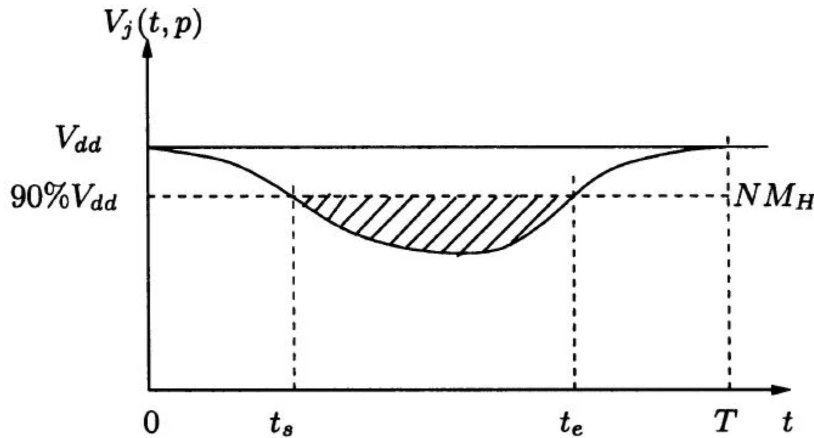


1. Image Li, Hang, et al. "Partitioning-based approach to fast on-chip decoupling capacitor budgeting and minimization." Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on 25.11 (2006): 2402-2412.

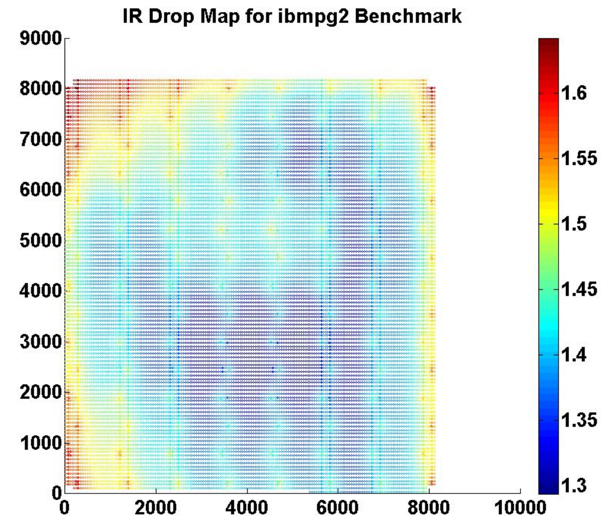
Electrical Representation of IC Power Grid[1]

- Supplies power to ICs
- Components:
  - C4 Bumps – Ideal Power Source with an inductor and resistor
  - Transistors – Current source
  - Decoupling Capacitances
  - Interconnect – Resistors

Power Supply Network Constraints



As transistors turn on the transient voltage droops



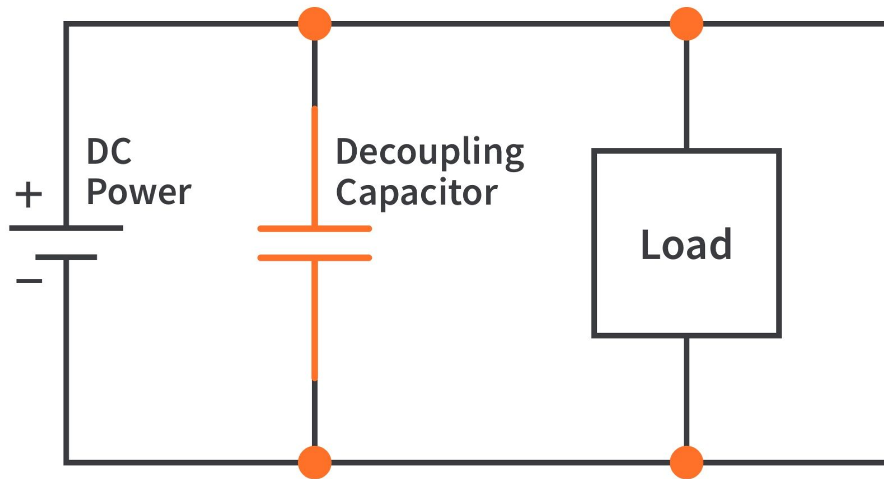
Dimensions in µm and colorbar in Volts. Low Voltages might lead to timing problems

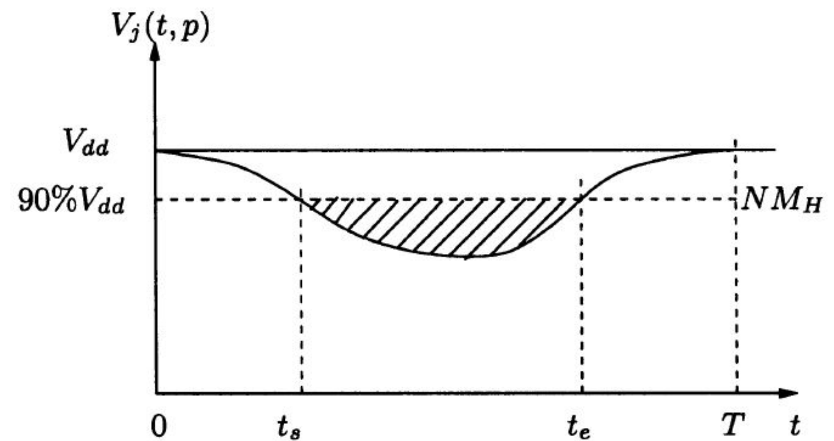
- Voltage Droop: All node transient voltages have to be above a specified threshold
- Static IR Drop: All node voltages have to be above a specified threshold
- Electromigration: Current constraint on interconnect

OpenLane Power Density

Decoupling Capacitance

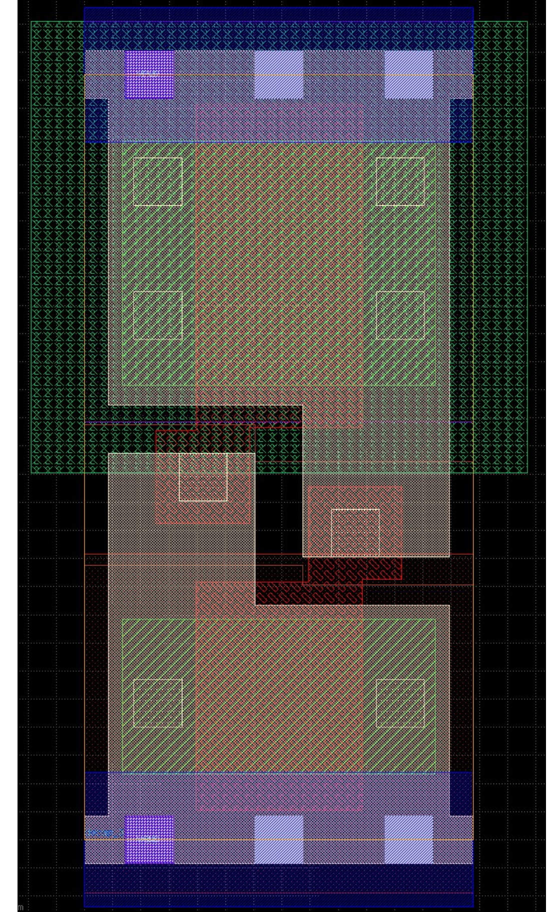
- Capacitor supplies power during transition periods until DC power can “catch up”
  - Size based on charge, frequency, etc.
- Often used in board-level design





Sky130 Decap Cells

LI-Poly-Diff Cap

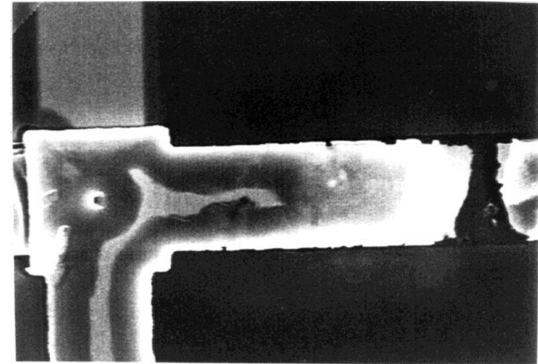


Today's Lecture

- Metal Density
- Antenna Checks
- Latch-Up
- IR Drop/Decoupling Capacitance
- Electromigration

Electromigration

- Two parts
  - "Hillocks" cause shorts
  - "Voids" cause opens
- Factors
  - Wire material
  - Temperature
  - Wire size
  - Current (peak, avg, RMS)



Electromigration in IC interconnect, a byproduct of large chip interconnect currents/temperatures.

Image from http://cc.ee.ntu.edu.tw/~ywchang/Courses/Vlsi2k/pictures.html.

Next Lecture

- Design for Manufacturing