Lecture 11: Interconnect

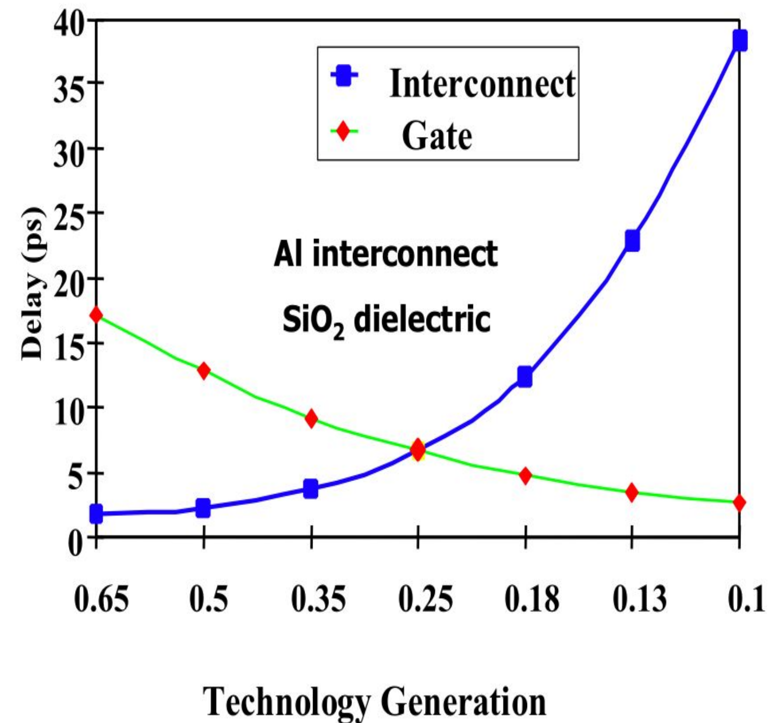
Matthew Guthaus
Professor
UCSC, Computer Science & Engineering
http://vlsida.soe.ucsc.edu
mrg@ucsc.edu

Today's Lecture

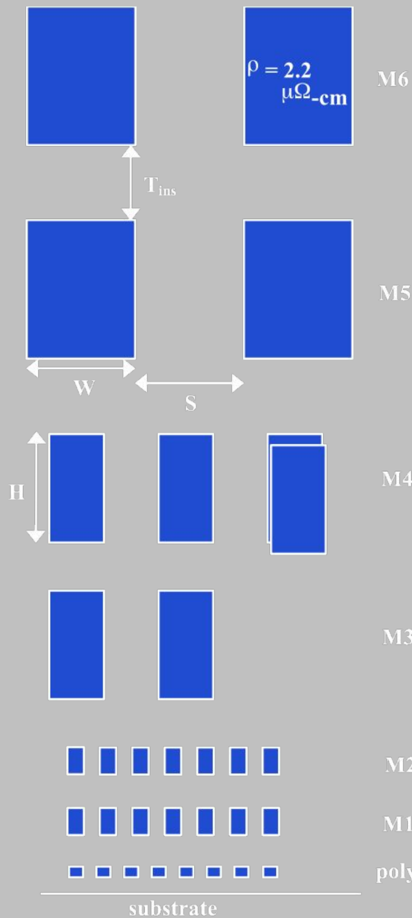
- Wiring or interconnections and their performance impact
  - Contribute to delay, RC
  - Coupling capacitance between wires
- Interconnect variation

Reverse Scaling of Interconnects

- Gate delays reduce with technology scaling
- Global interconnect delays increase with scaling
  - Interconnects must be included in analysis and optimization

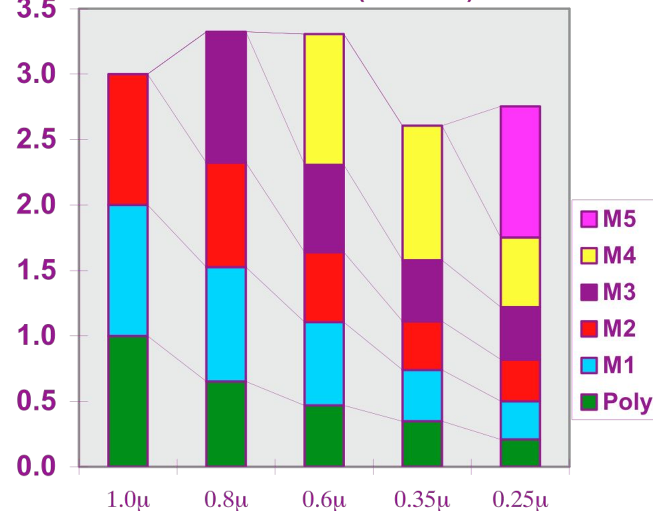


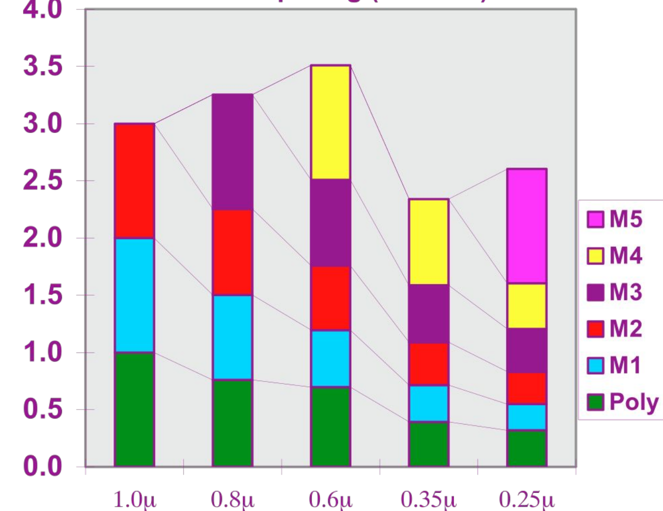
Interconnect: # of Wiring Layers



of metal layers is steadily increasing due to:

- Increasing die size and device count: we need more wires and longer wires to connect everything
- Rising need for a hierarchical wiring network; local wires with high density and global wires with low RC





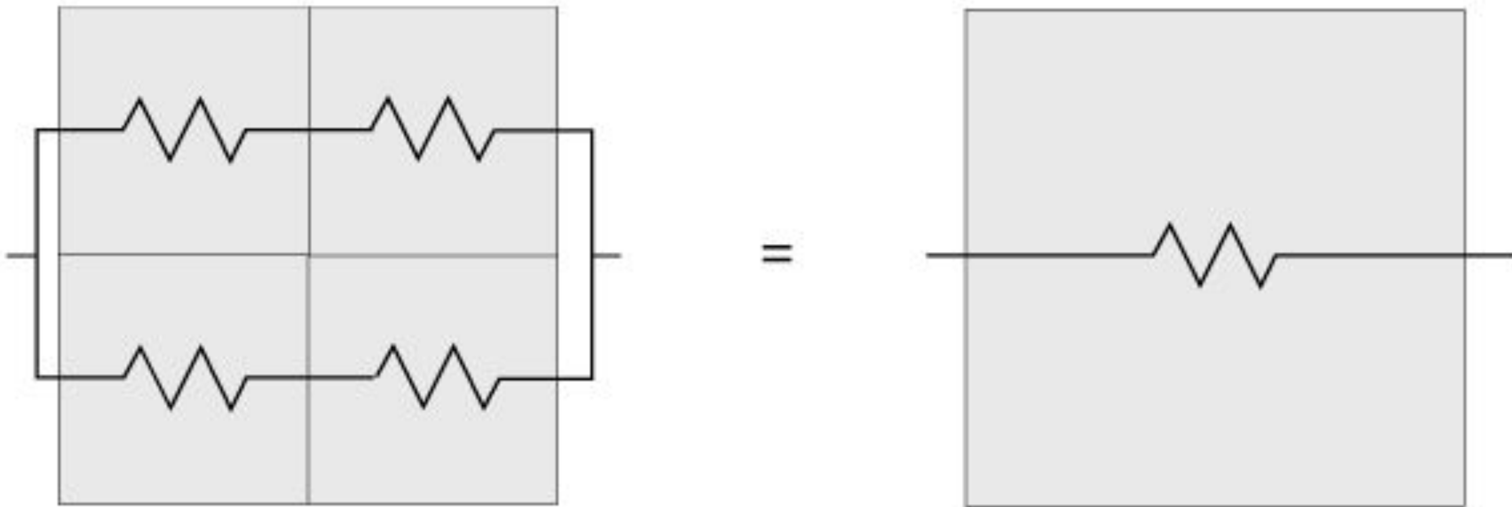
Interconnect Parasitics

- Classes of parasitics
  - **Capacitance**
  - **Resistance**
  - Inductance
- Impact of interconnect parasitics
  - Increases propagation delay
  - Energy dissipation and power distribution
  - Reliability and signal integrity

Wire Resistance

Resistance of any “square” is roughly constant

Key: thickness is the same



$R_{\square} * L/W$

Sheet Resistance of Materials

Representative

Material	Sheet Resistance (Ω/❑)
n- or p-well diffusion	1000 – 1500
n^+, p^+ diffusion	50 – 150
n^+, p^+ diffusion with silicide	3 – 5
n^+, p^+ polysilicon	150 – 200
n^+, p^+ polysilicon with silicide	4 – 5
Aluminum	0.05 – 0.1

Table 91 Table - Resistances

Layer	Resistivity (mohms/sq)
Poly	48200
Local interconnect	12800
Metal1	125
Metal2	125
Metal3	47
Metal4	47
Metal5	29
Deep nwell	2200000
Pwell (in deep nwell)	3050000
Nwell	1700000
N-diffusion	120000
P-diffusion	197000
HV N-diffusion	114000
HV P-diffusion	191000
XHR poly resistor	319800
UHR poly resistor	2000000
LICON contact	15000
MCON contact	152000
VIA	4500
VIA2	3410
VIA3	3410
VIA4	380

Sky130 (note mohms)

Sky130 Resistances

Split into two to be visible

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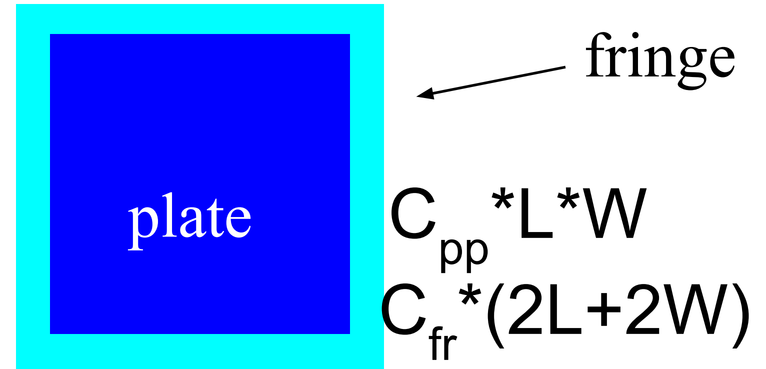
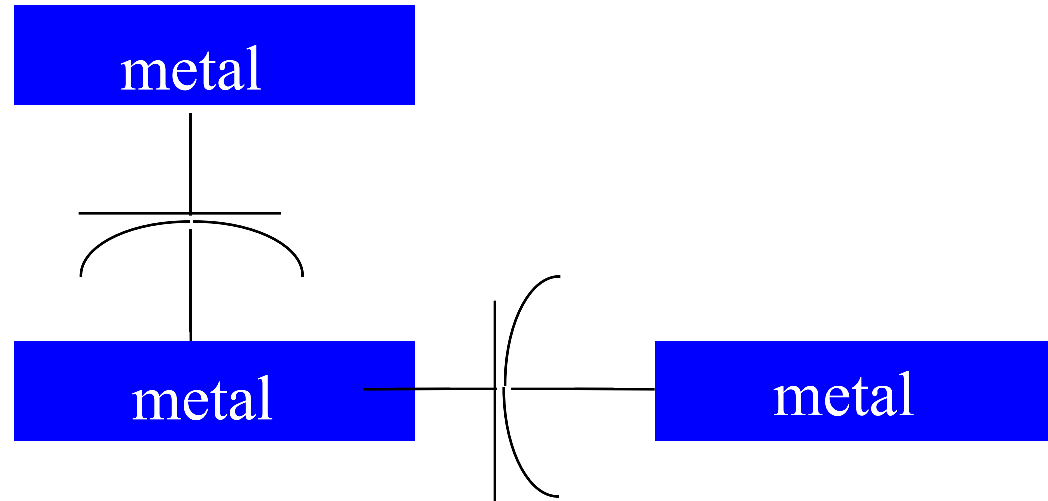
Wire Capacitance

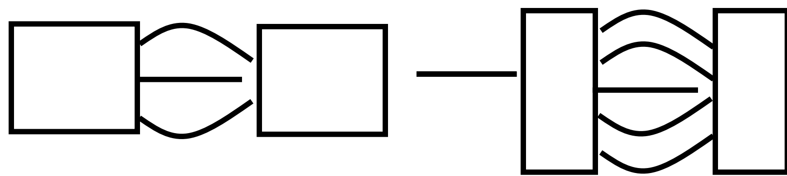
- Two components
  - Parallel plate cap.
  - Fringe cap.
  - Units per mm usually
- Coupling
  - Intra-layer
  - Inter-layer



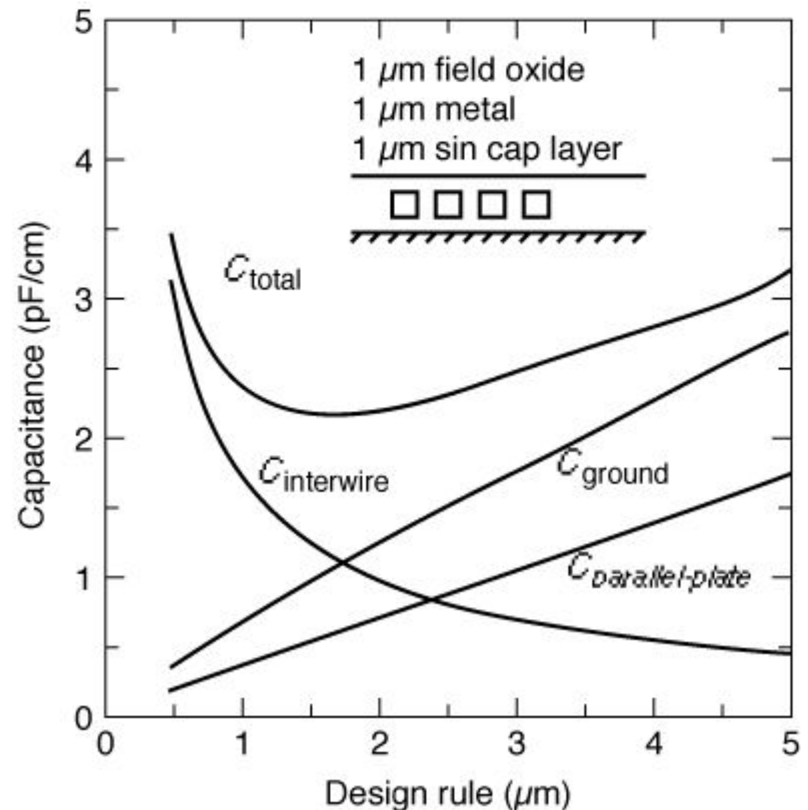


Coupling Capacitance

- To reduce interconnect resistance, thickness is not scaled as aggressively as the width of the interconnect



- Tall wires (high aspect ratios)
- ~2.4 in 90nm



Sky130 Capacitances

NOTE: Adjacent capacitance depends on spacing! This will be done by “extraction”.

Basic Capacitance - Parallel

Table 95 Table - Capacitance - Parallel

Interlayer parallel plate capacitance (aF/um^2)	Local interconnect	Metal1	Metal2	Metal3	Metal4	Metal5
Poly	94.1644	44.8056	24.4968	16.0552	10.0131	7.2085
Local interconnect		114.1970	37.5647	20.7915	11.6705	8.0265
Metal1			133.8610	34.5350	15.0275	9.4789
Metal2				86.1861	20.3321	11.3410
Metal3					84.0346	19.6269
Metal4						68.3252

Table 94 Table - Capacitance - Fringe Upward

Interlayer fringe capacitance (upward direction) (aF/um)	Local interconnect	Metal1	Metal2	Metal3	Metal4	Metal5
Poly	25.138	16.691	11.166	9.18	6.3505	6.4903
Local interconnect		34.7	21.739	15.078	10.141	7.6366
Metal1			48.193	26.676	16.421	12.017
Metal2				44.432	22.332	15.693
Metal3					42.643	27.836
Metal4						46.976

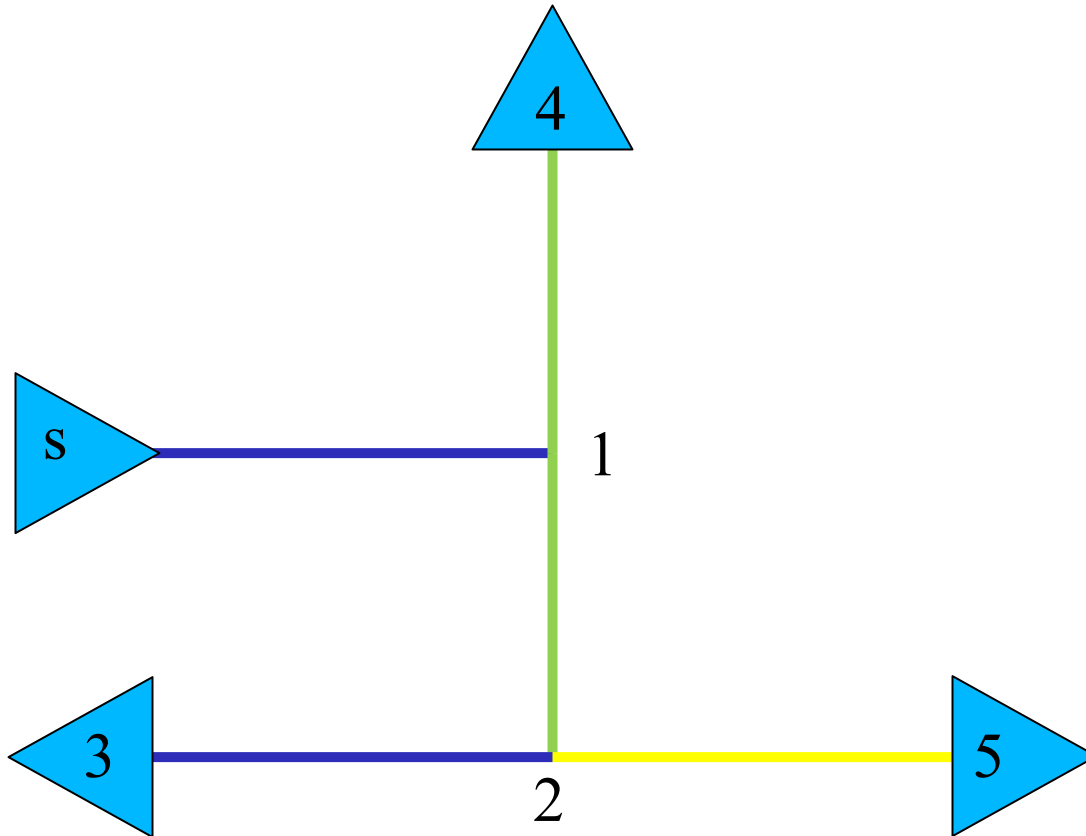
Table 93 Table - Capacitance - Fringe Downward

Interlayer fringe capacitance (downward direction) (aF/um)	Poly	Local interconnect	Metal1	Metal2	Metal3	Metal4
Local interconnect	51.846					
Metal1	46.724	59.496				
Metal2	41.222	46.277	67.045			
Metal3	43.531	46.708	54.814	69.846		
Metal4	38.105	39.709	42.563	46.382	70.522	
Metal5	39.908	41.147	43.188	45.592	54.152	82.819

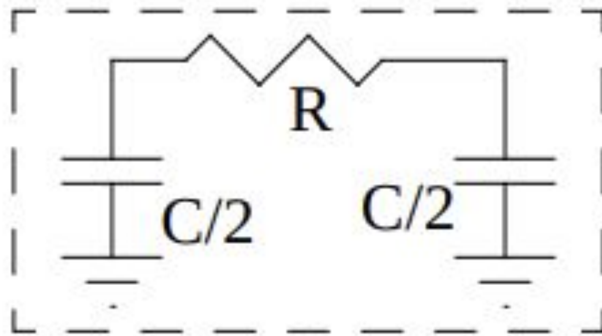
Interconnect Modeling: Elmore Again!

- Lumped capacitance model is what we use for device/gate analysis
- Lumped RC model
  - For simple one segment RC:
    - 50% Delay = 0.69*RC
    - 10-90% Slew = 2.2*RC
- Distributed RC line model
  - More accurate for interconnect analysis
    - 50% Delay = 0.38*RC
    - 10-90% Slew = 0.9*RC

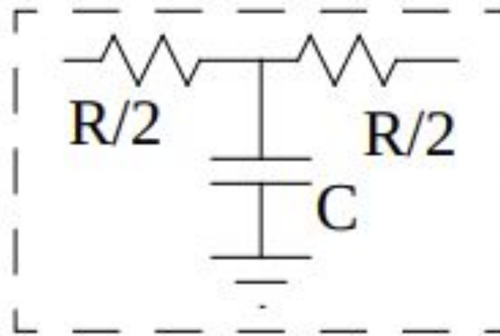
Interconnect Delay



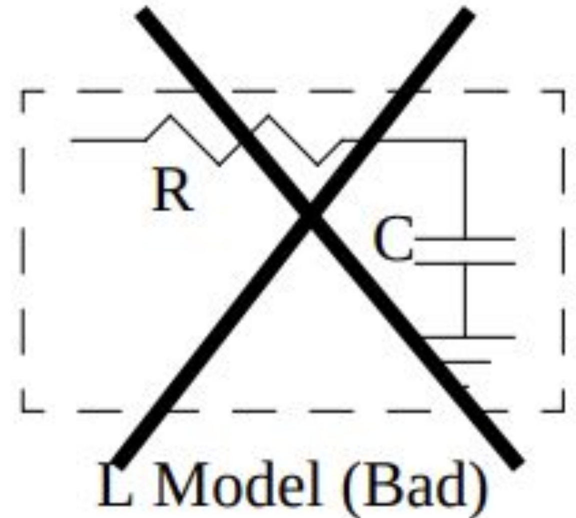
Equivalent Wire Models



Pi Model

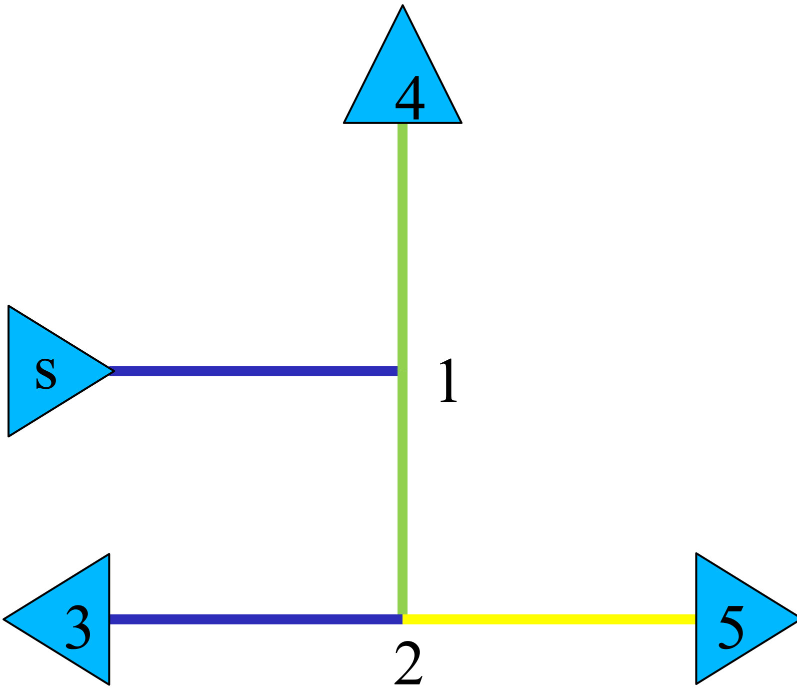


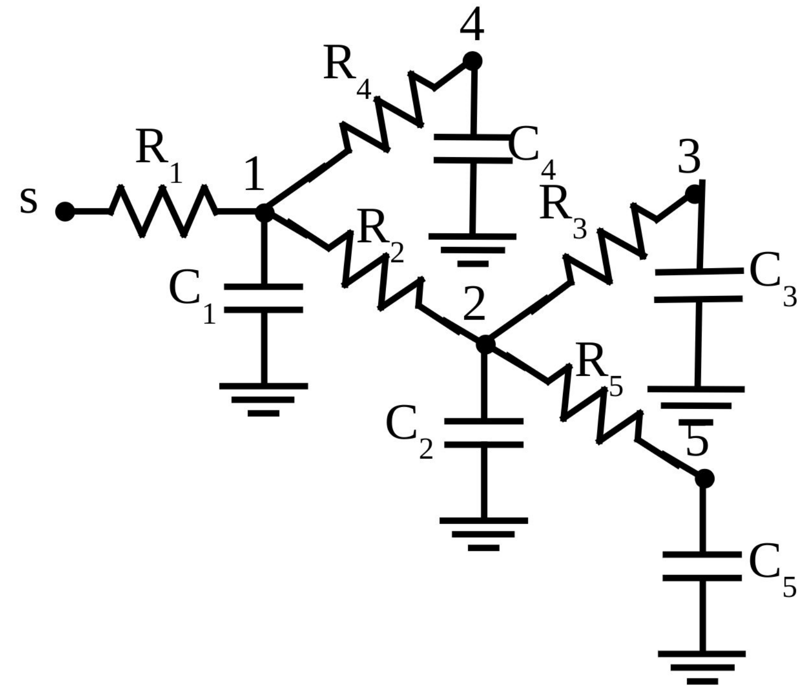
T Model



L Model (Bad)

Wire Delay Modeling





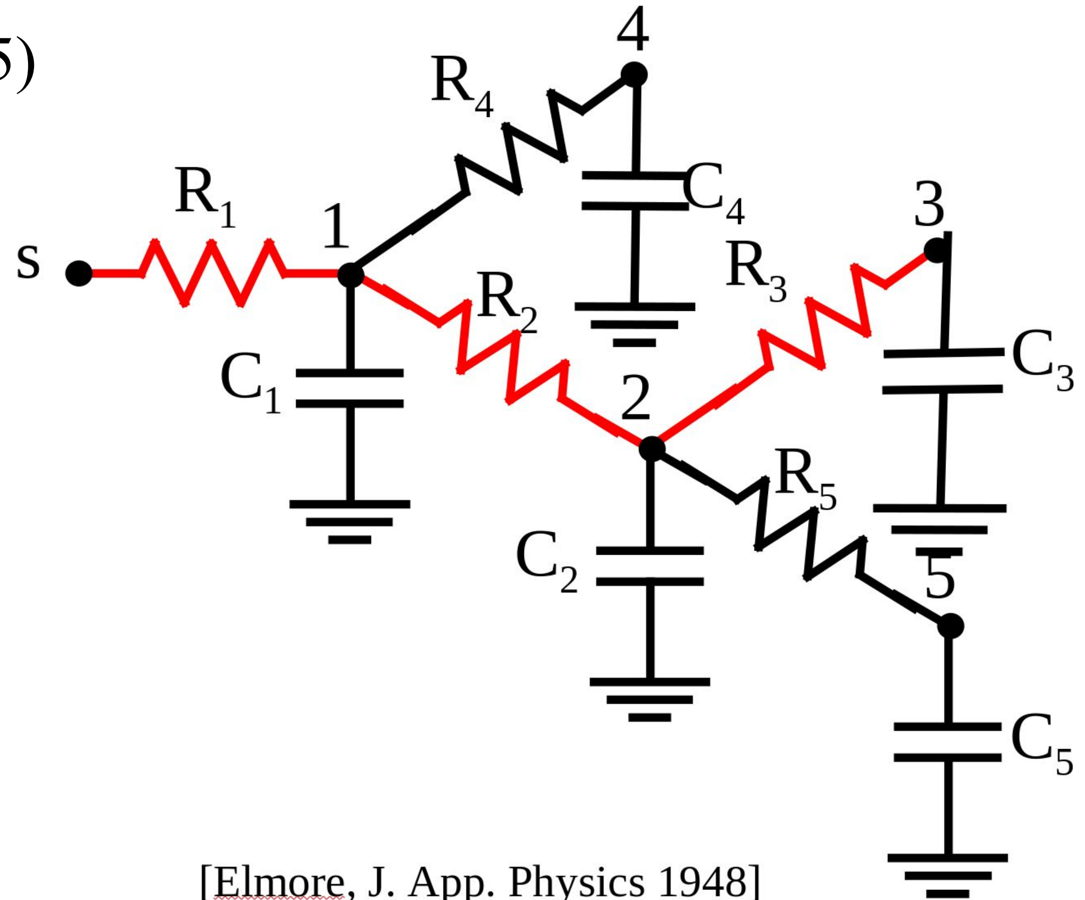
Elmore Delay Calculation

Method 1: per resistor

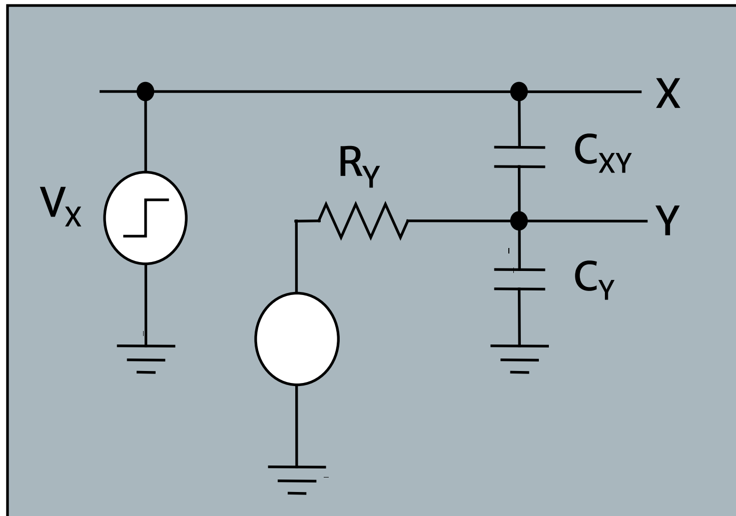
0.69*(R1(C1+C2+C3+C4+C5)
+ R2(C2+C3+C5)
+R3C3)

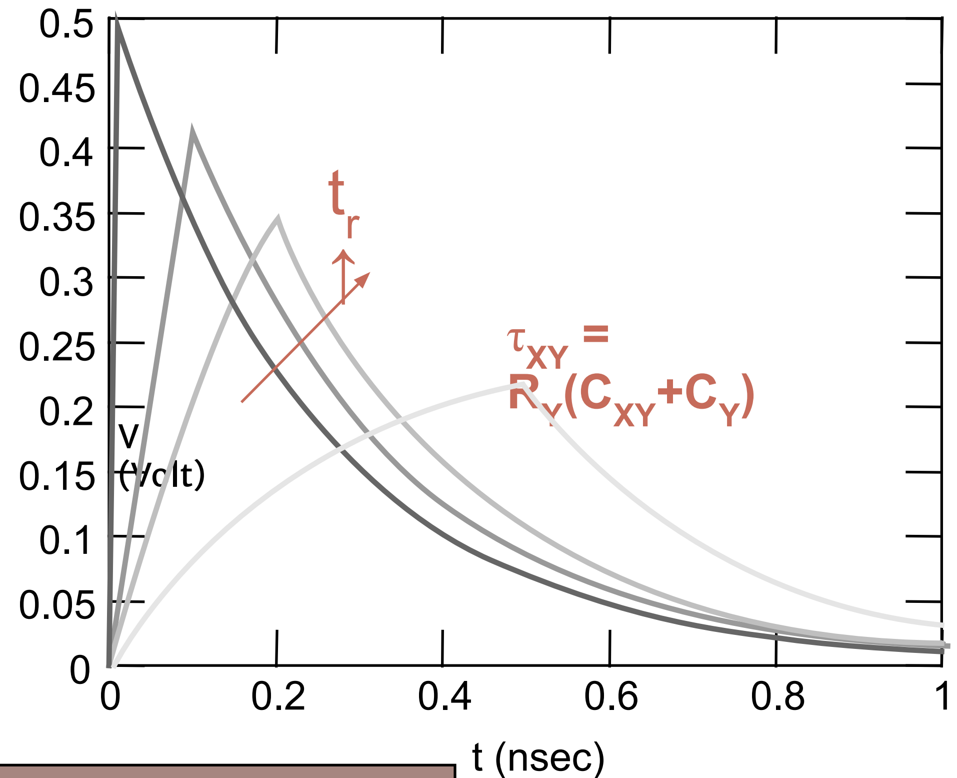
Method 2: per capacitor

0.69*(R1C1
+(R1+R2)C2
+(R1+R2+R3)C3
+R1C4
+(R1+R2)C5)



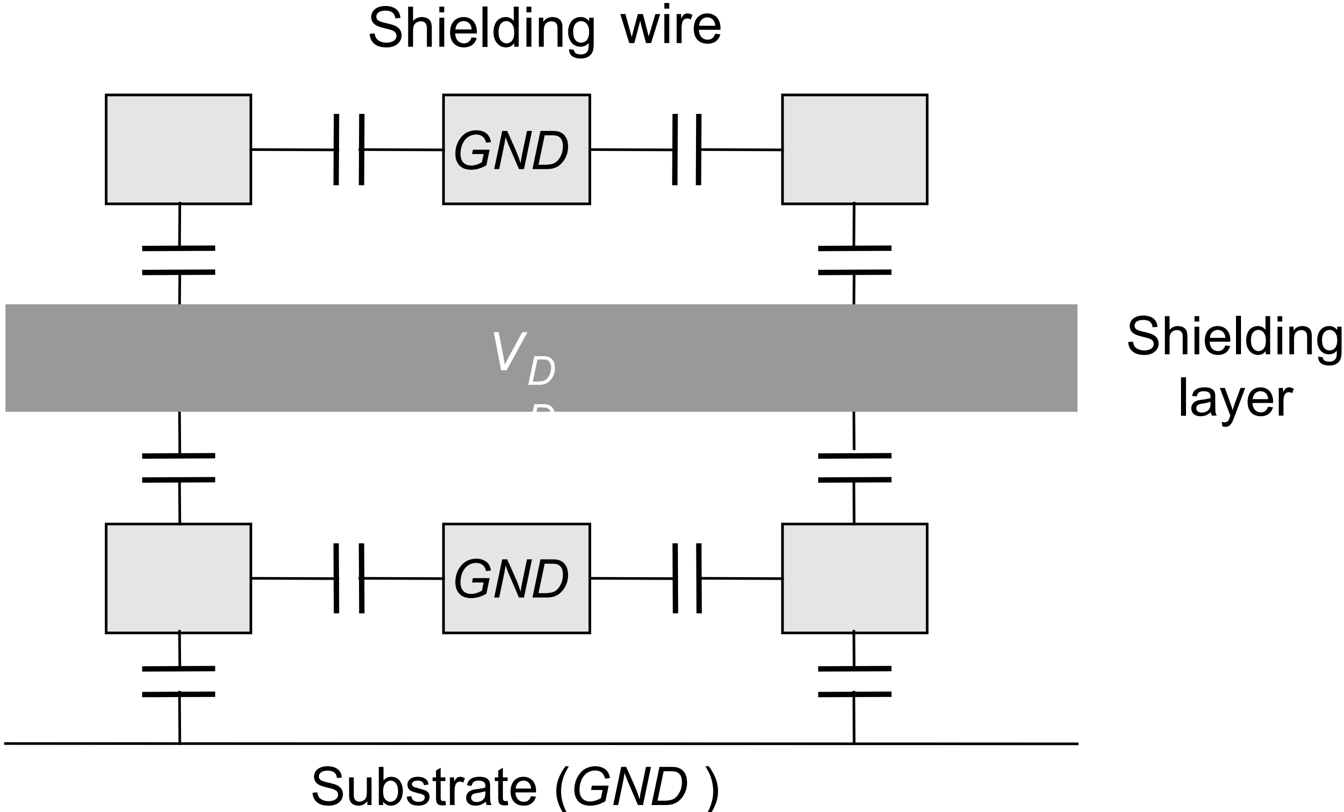
Challenge: Capacitive Cross Talk





$$\Delta V_Y = \frac{C_{XY}}{C_Y + C_{XY}} \Delta V_X$$

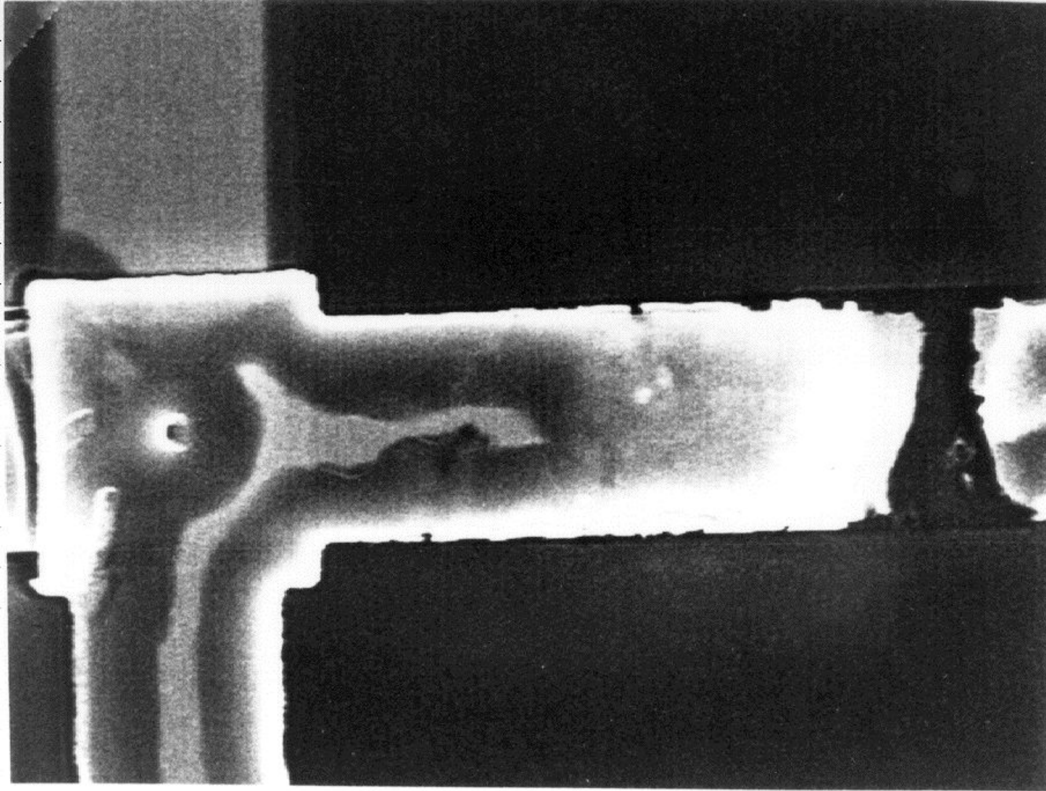
Shielding



Wiring problems

- Diffusion: changes in doping means variations in resistance, capacitance.
- Poly, metal: variations in height, width means variations in resistance, capacitance.
- Shorts and opens during manufacturing

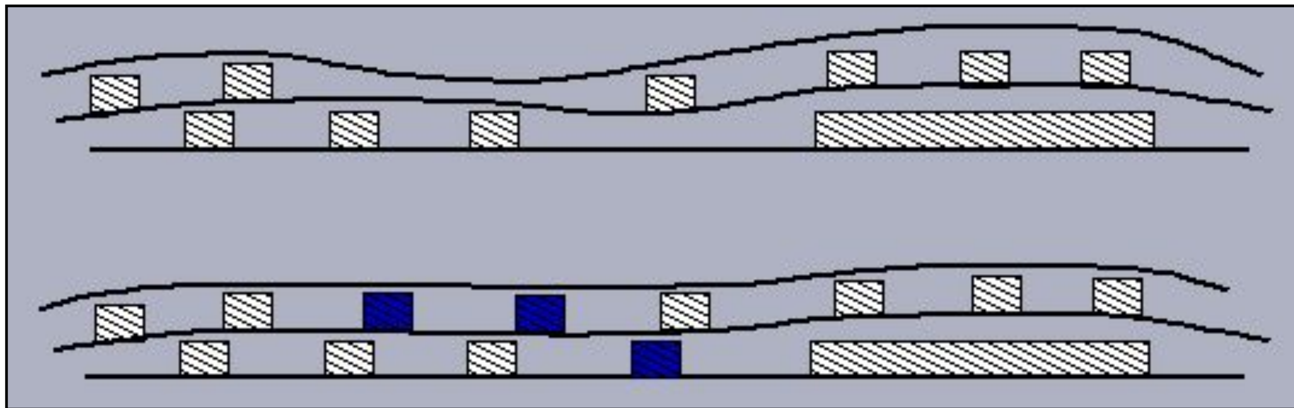
Electromigration



Oxide and Metal Thickness Variation

Due to Chemical Mechanical Polishing (CMP)

More when we talk about “chip finishing”...



Next Lecture

- See handout