Lecture 10: Gate Delay and Power

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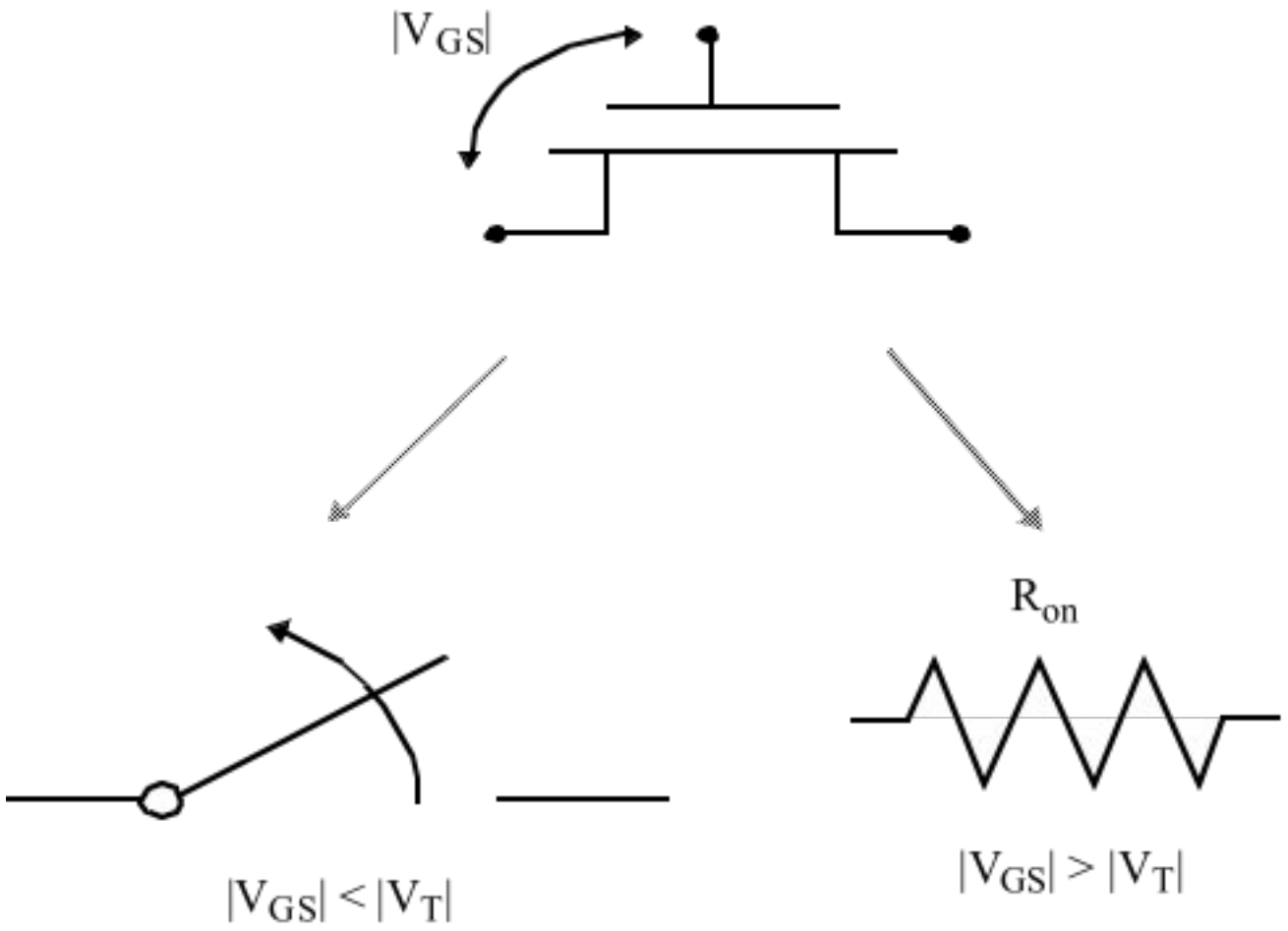
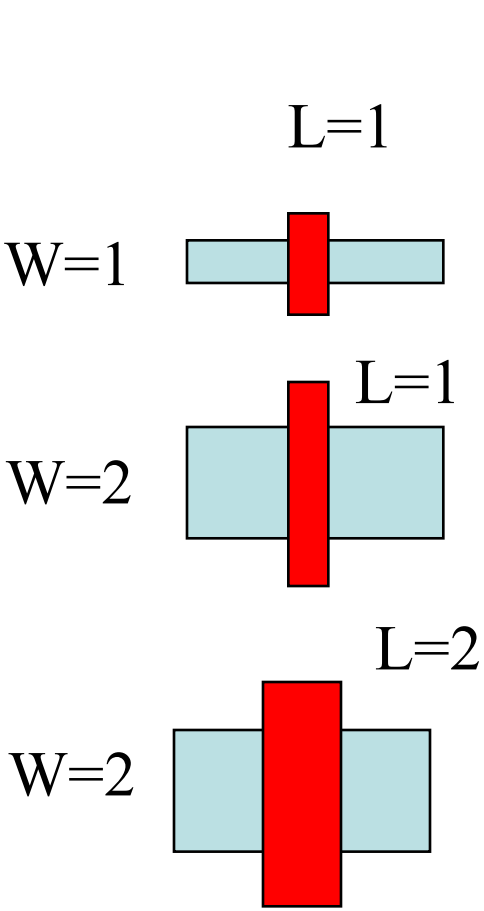
Today's Topics

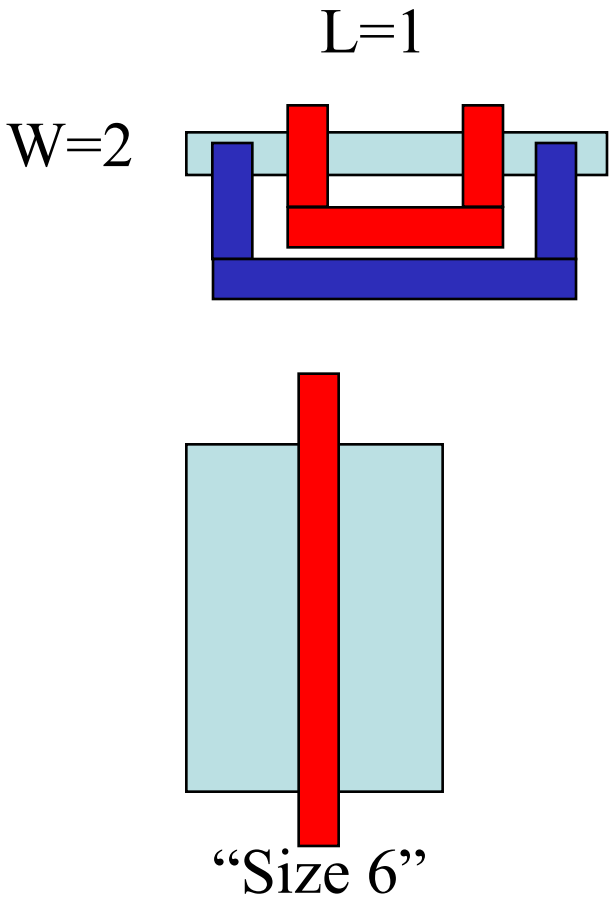
- Switched transistor networks
- First-order gate delay model
  - Elmore Delay
- Power consumption

Switch Model… Again



Transistor W and L

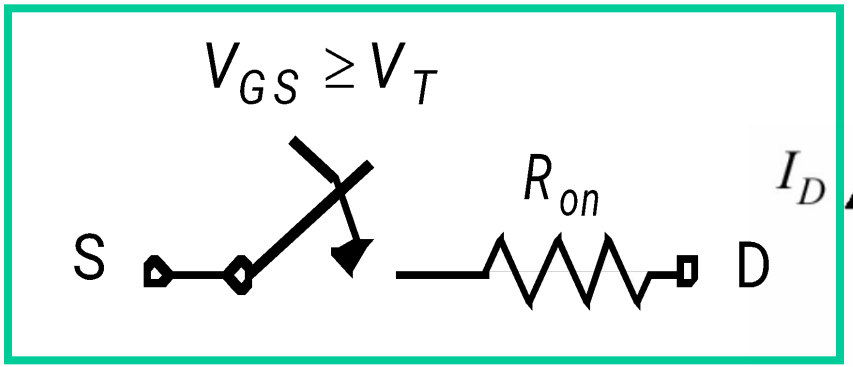


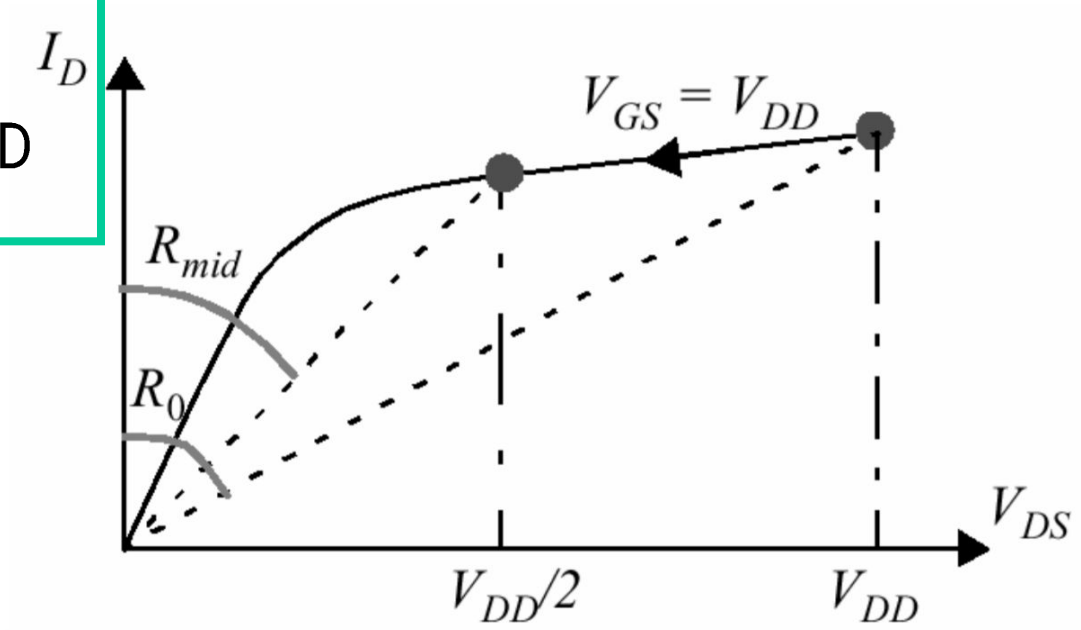


"Size 6"

Size is often compared to minimum.

Transistor as a Switch… Again





Resistors should be linear, right?

R = Vds / Id
Ron ≅ average(R0, Rmid)

Req ∝ L/W

Req, W, and L

Resistance goes up as L goes up

"Resistance in series"

Resistance goes down as W goes up

"Resistance in parallel"

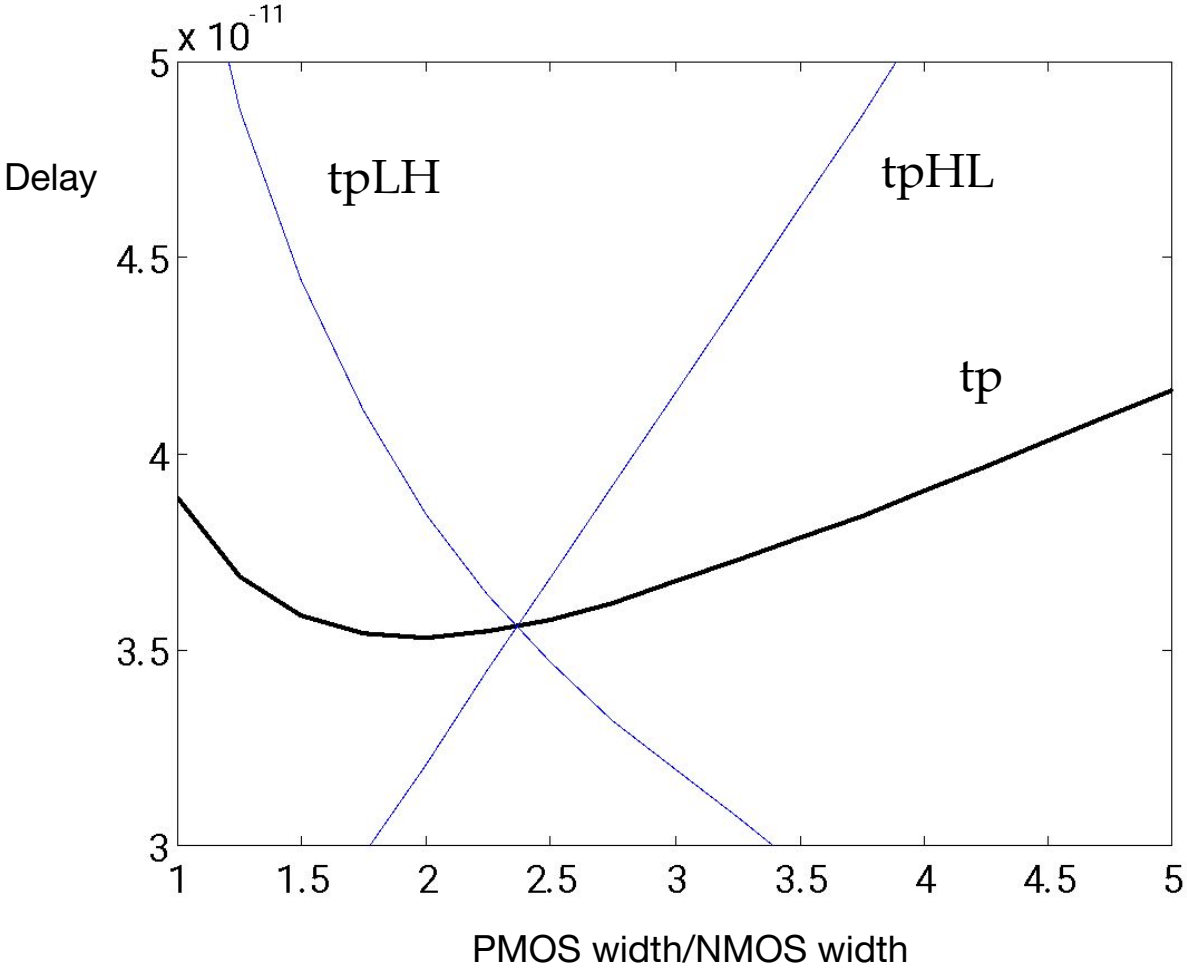
Req is proportional to L/W

Each transistor will have a W and L, if L is not given, it is minimum.

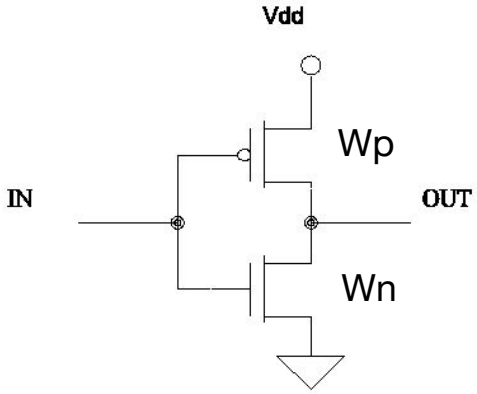
$$Req \propto L/W$$

PMOS vs NMOS Resistance

Vary “ratio” of PMOS to NMOS width



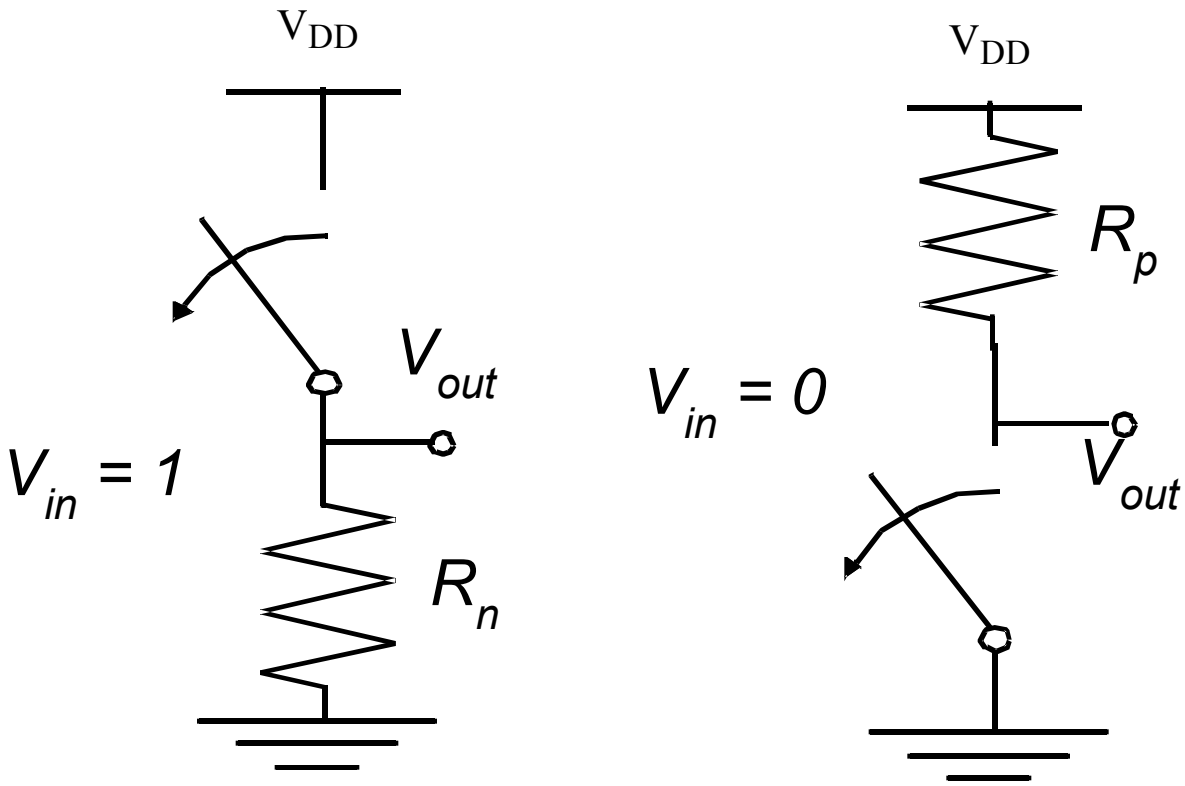
$$\beta = W_p / W_n$$



Relative resistances

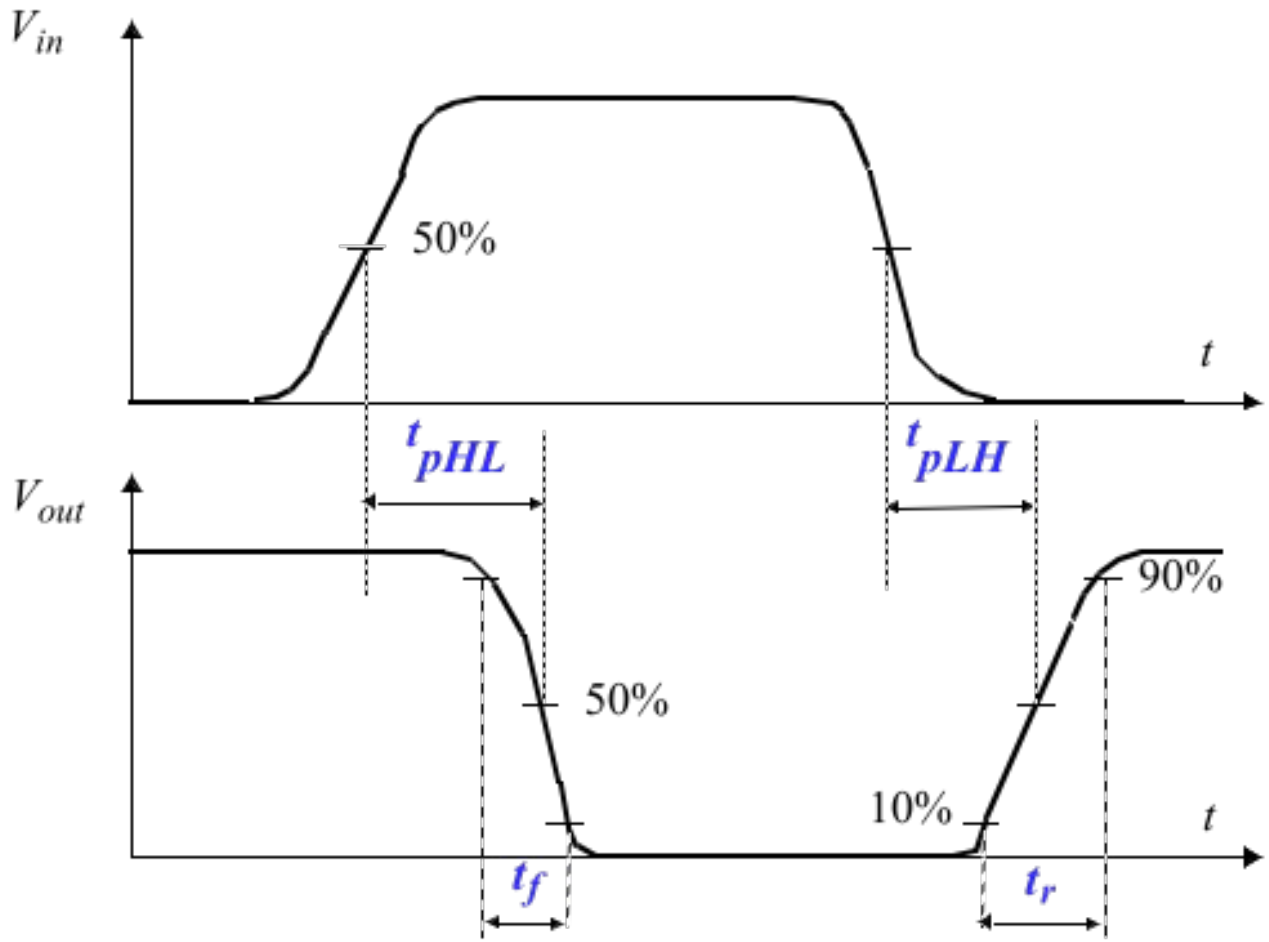
- We often don't need R explicitly, but instead know that:
  - 2W has half the R of W
  - 4W has ¼ the R of W
  - etc.
- Device types
  - PMOS is twice the R of same size NMOS
  - PMOS of size 2W is same R as NMOS of size W

First Order (Static) Analysis



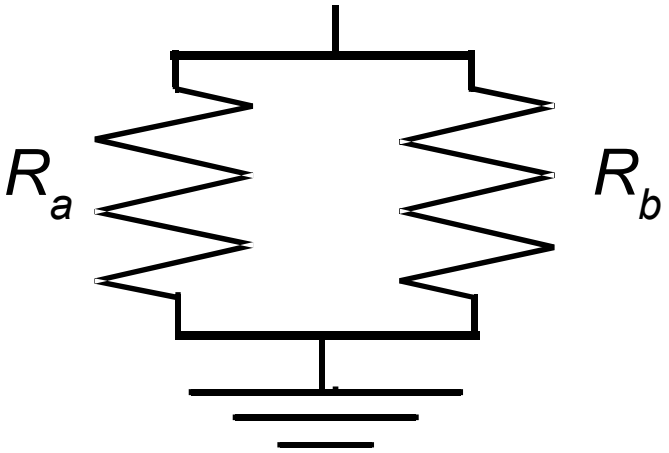
$V_{OL} = 0$
$V_{OH} = V_{DD}$
$V_M = f(R_n, R_p)$

Delay vs Rise/Fall Definitions



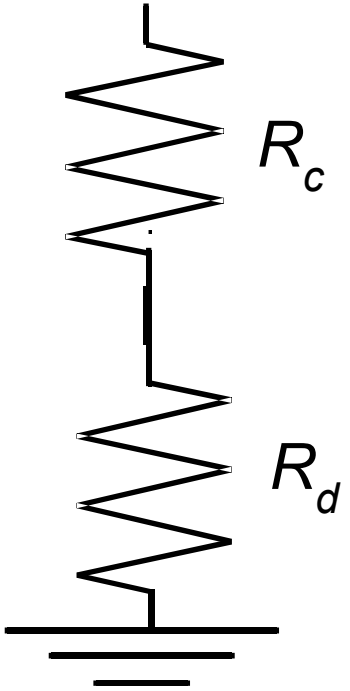
Switch Model

Which is faster? (Assume same size transistors)



$$1/R_{eq} = 1/R_a + 1/R_b$$

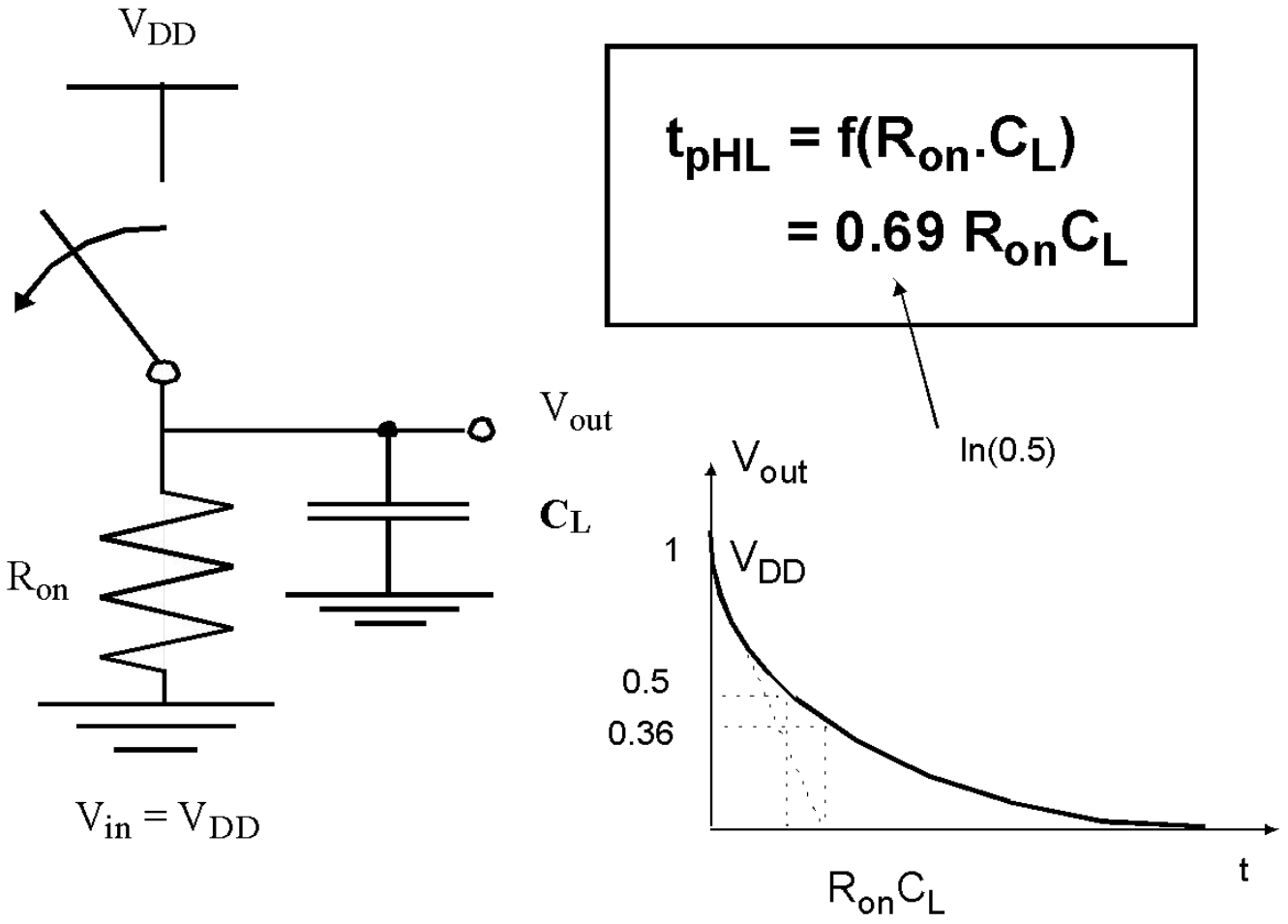
Sometimes double current



$$R_{eq} = R_a + R_b$$

Half the current

Transient (Elmore) Delay



Intuition Check

Delay = 0.69RC

What happens if you drive twice the fanout?

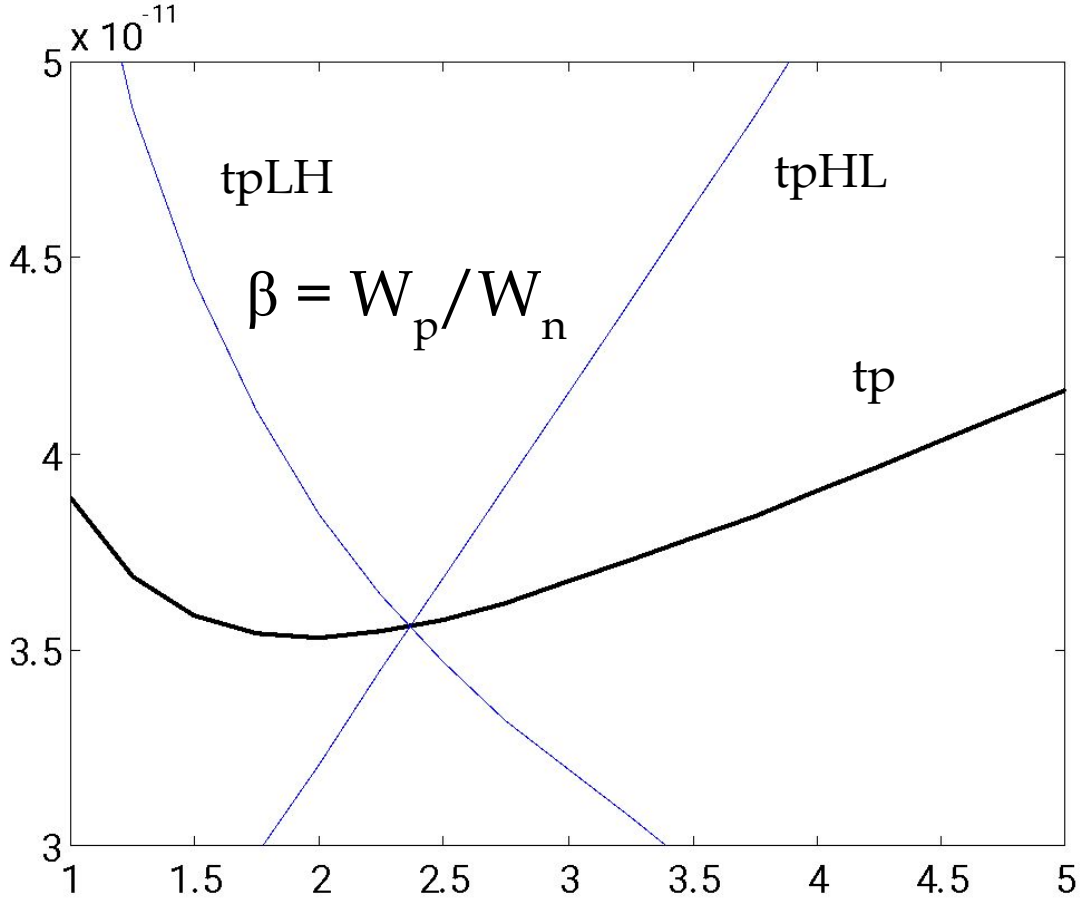
What happens if you use a “2x” gate instead of a “1x” (this is drive strength)?

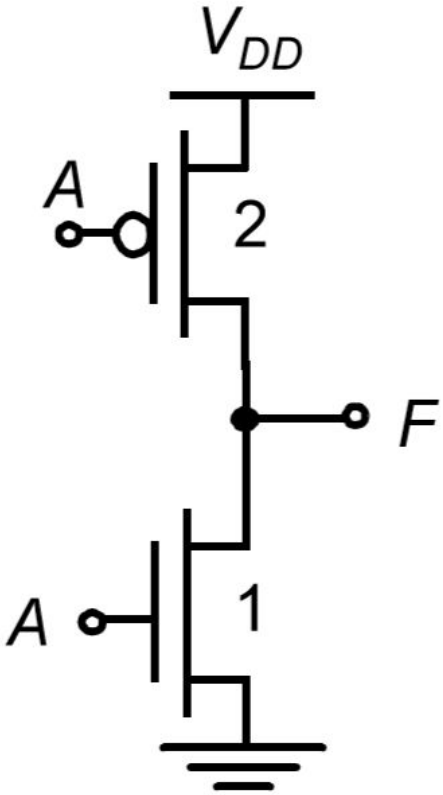
Pros/Cons of Elmore Delay

- Cons
  - Input is an ideal step
  - Assumes resistor model
  - Ignores short-circuit current
  - Output capacitance computation
    - Summing all the fanout and wires is pessimistic
    - Most tools use “effective capacitance”
- Pros
  - Simple and intuitive
  - Fast
  - Good fidelity, but not accuracy

PMOS vs NMOS Resistance

Vary “ratio” of PMOS to NMOS width

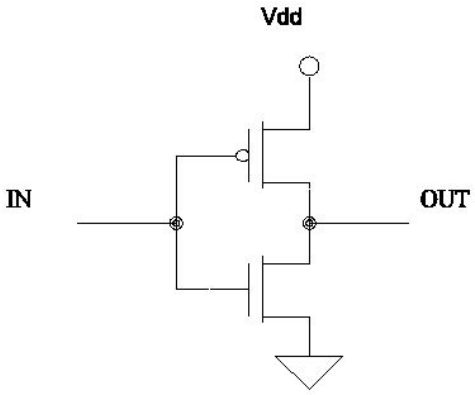


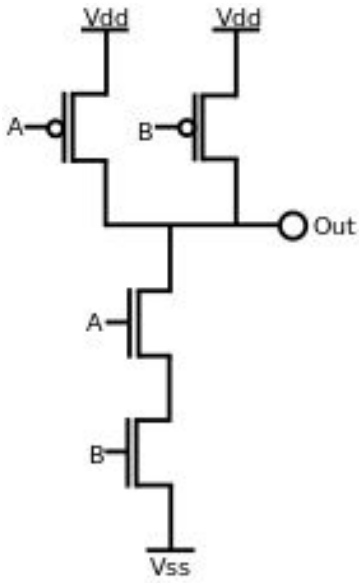


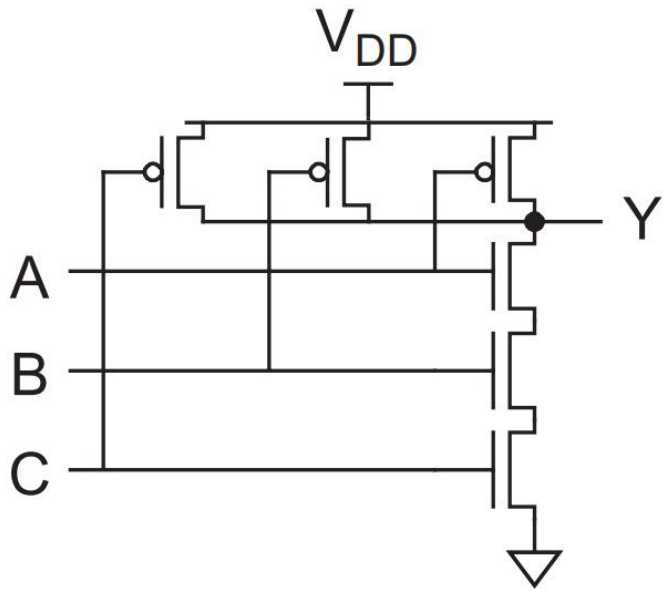
Scaling of NAND Delay

Series transistors in pull down add up resistance.

More series resistance means more delay.

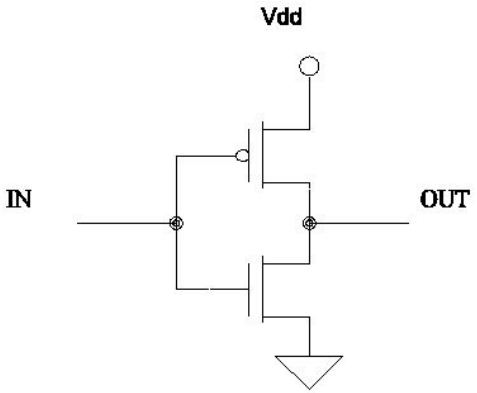


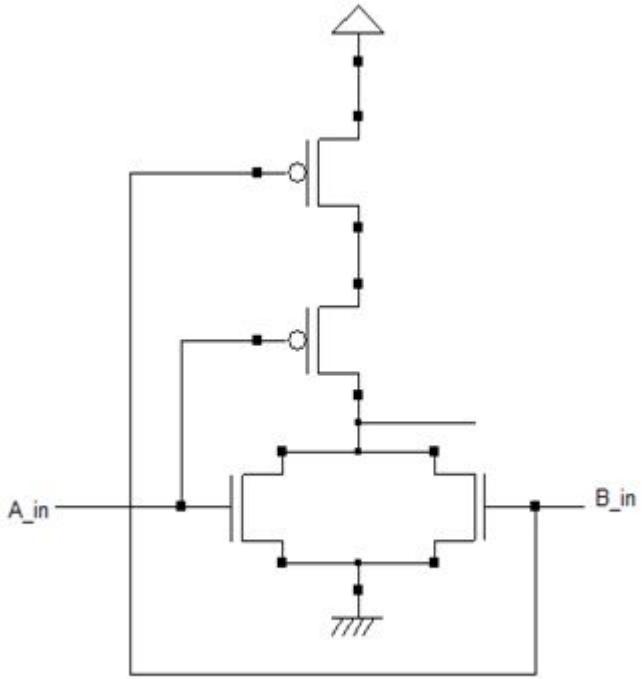


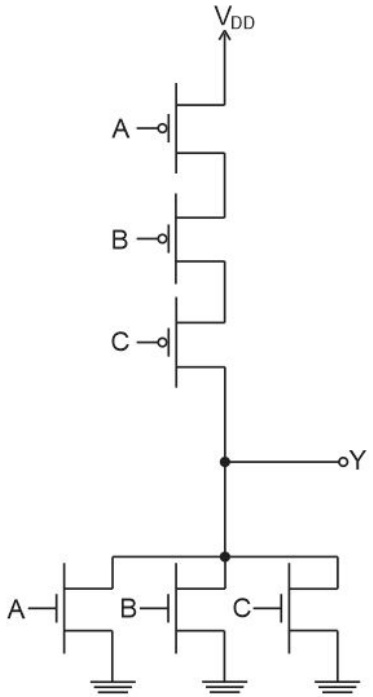


Scaling of NOR Delay

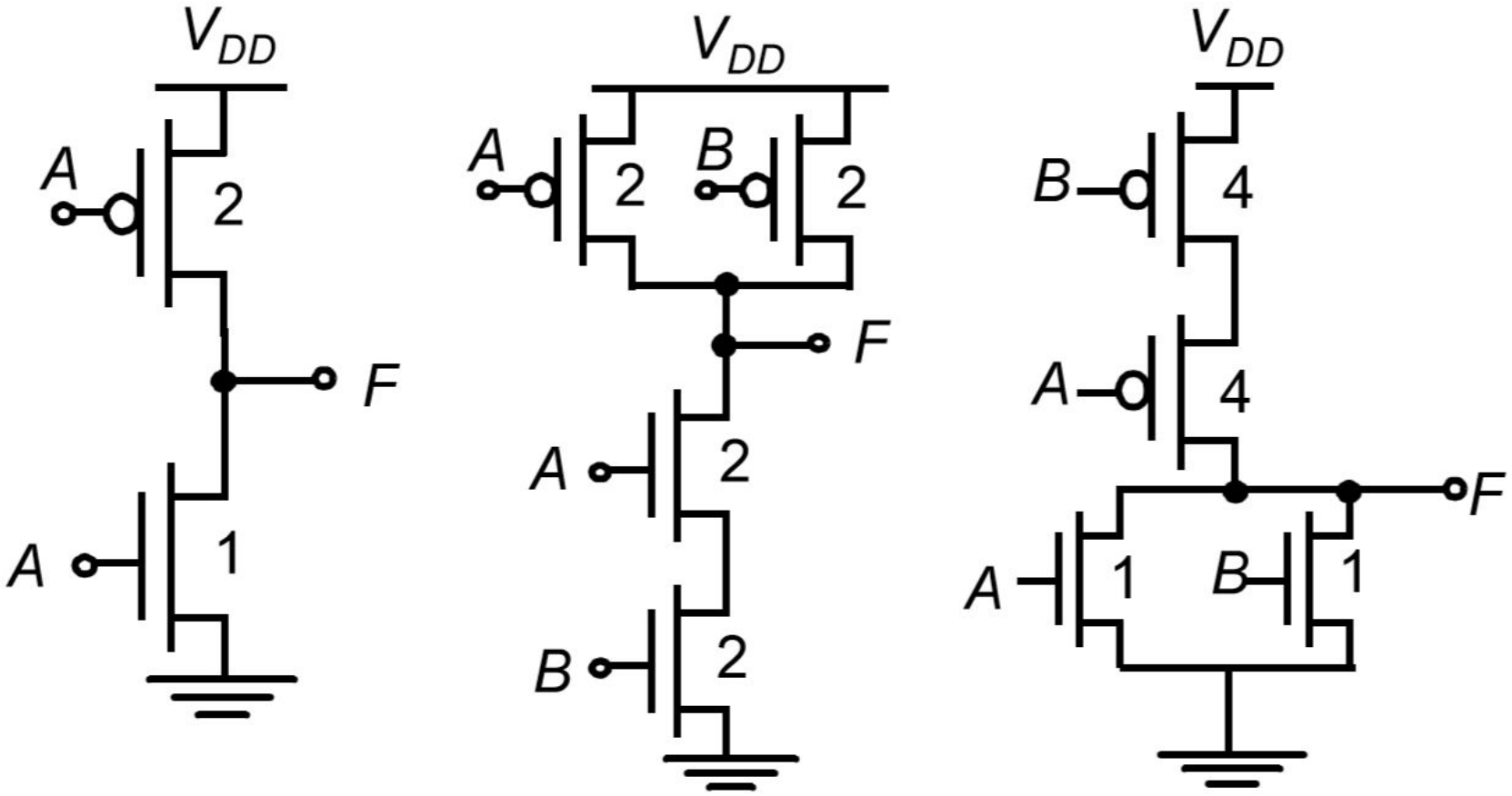
Similar to NAND, but pull up delay increases.





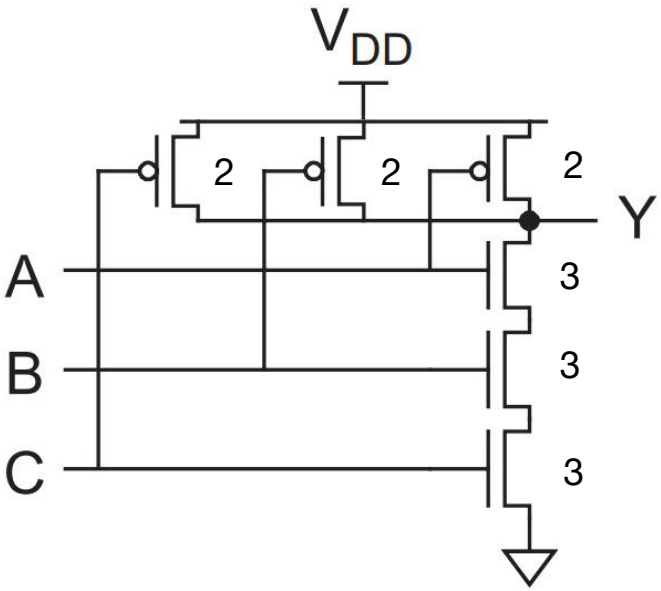


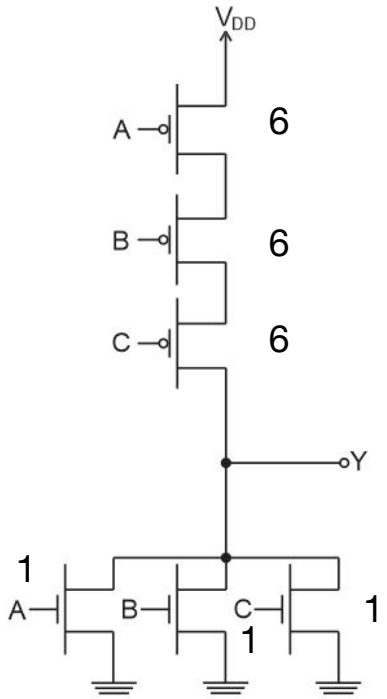
Equivalent Width Gates



Req ∝ L/W

NAND3 and NAND4

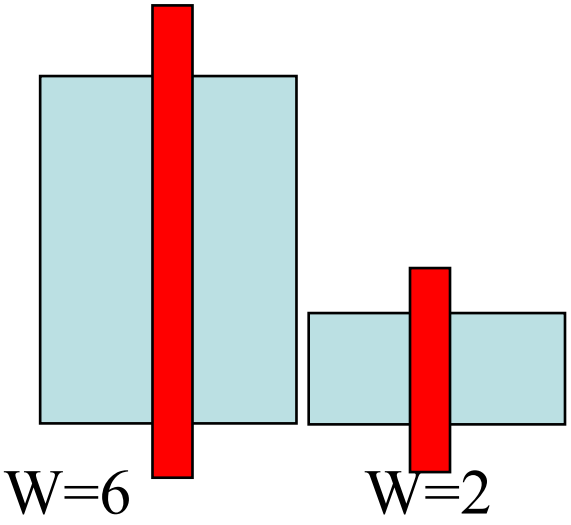


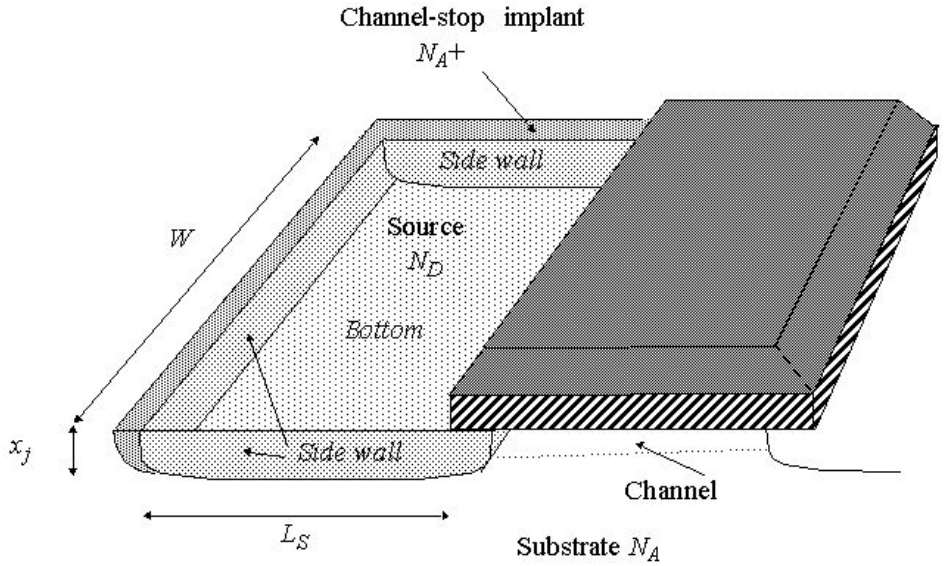


Diffusion Capacitance

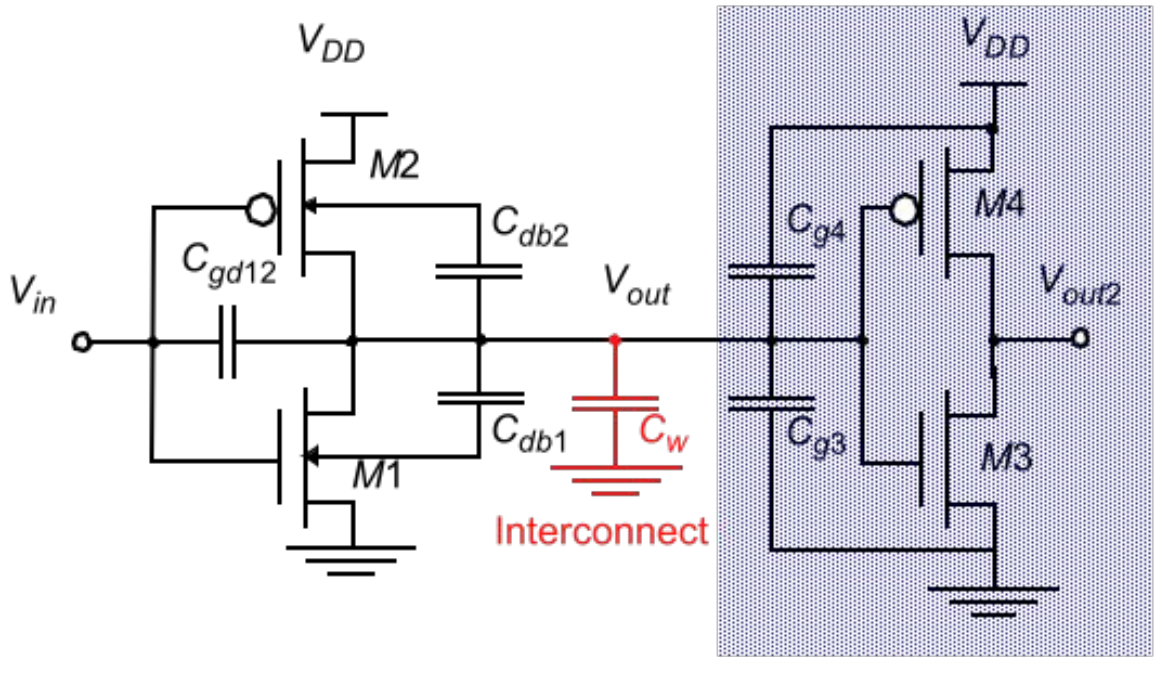
Diffusion capacitance proportional to transistor width

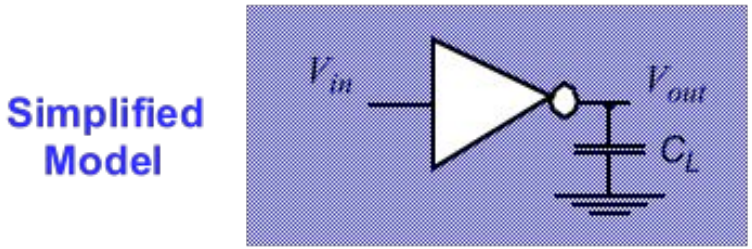
Capacitance related to perimeter and area



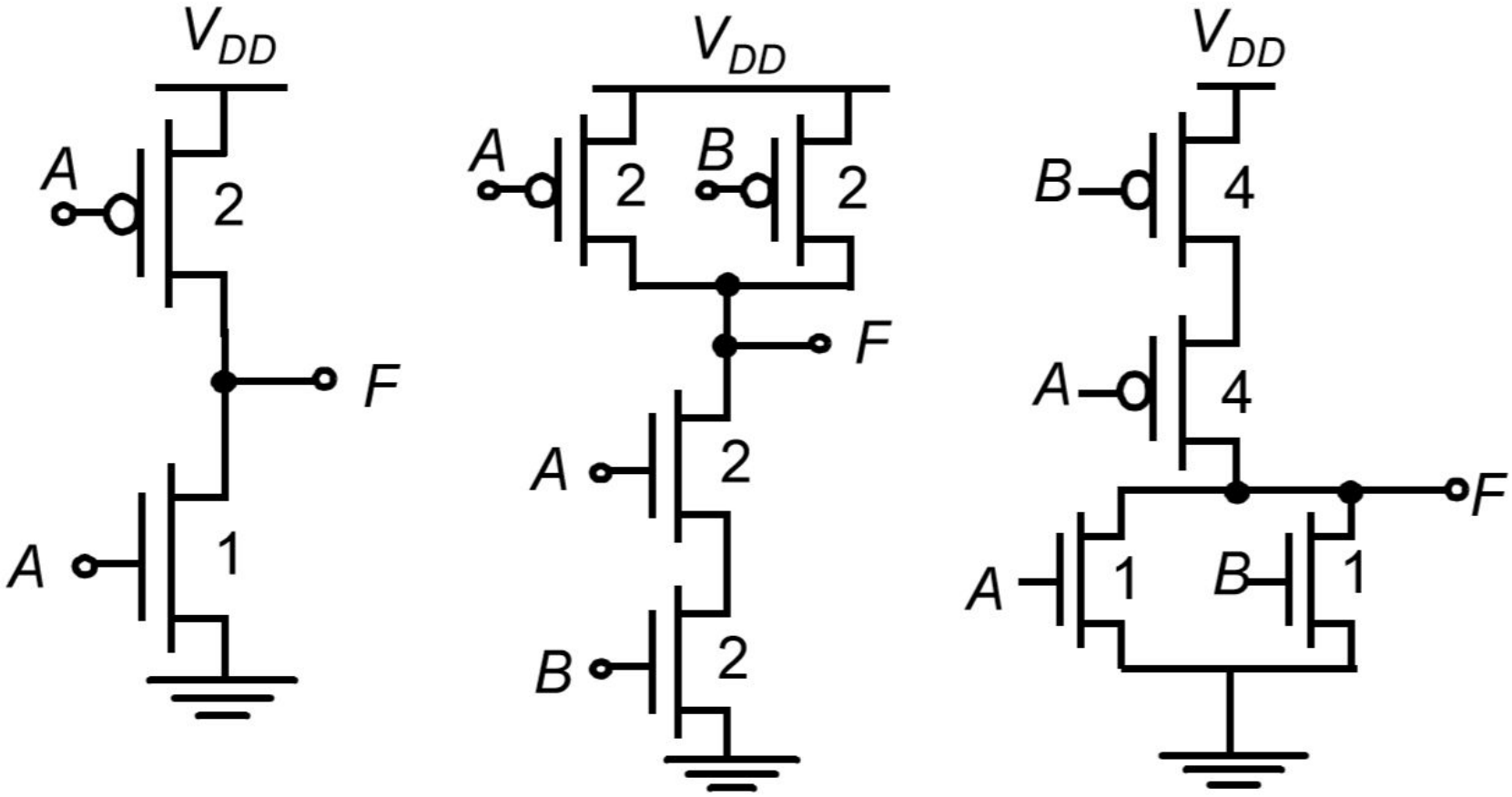


Visualizing the Capacitances

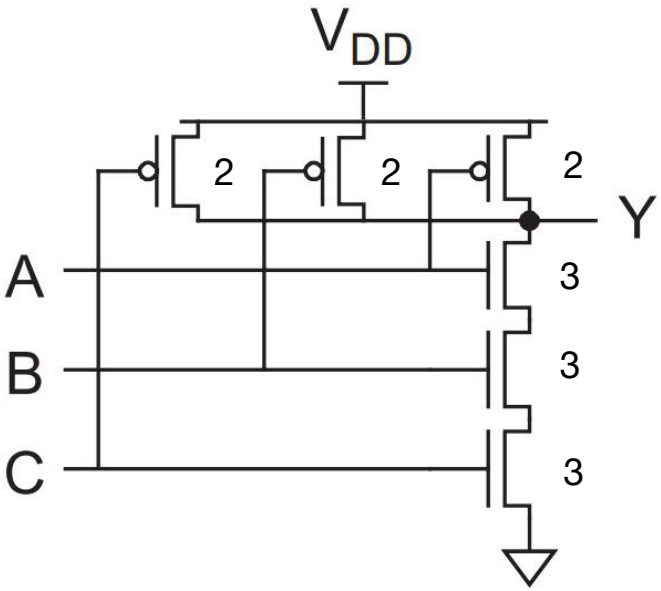


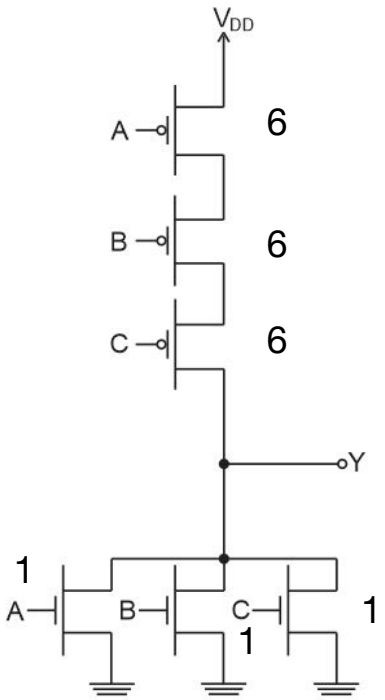


How much self-loading capacitance?



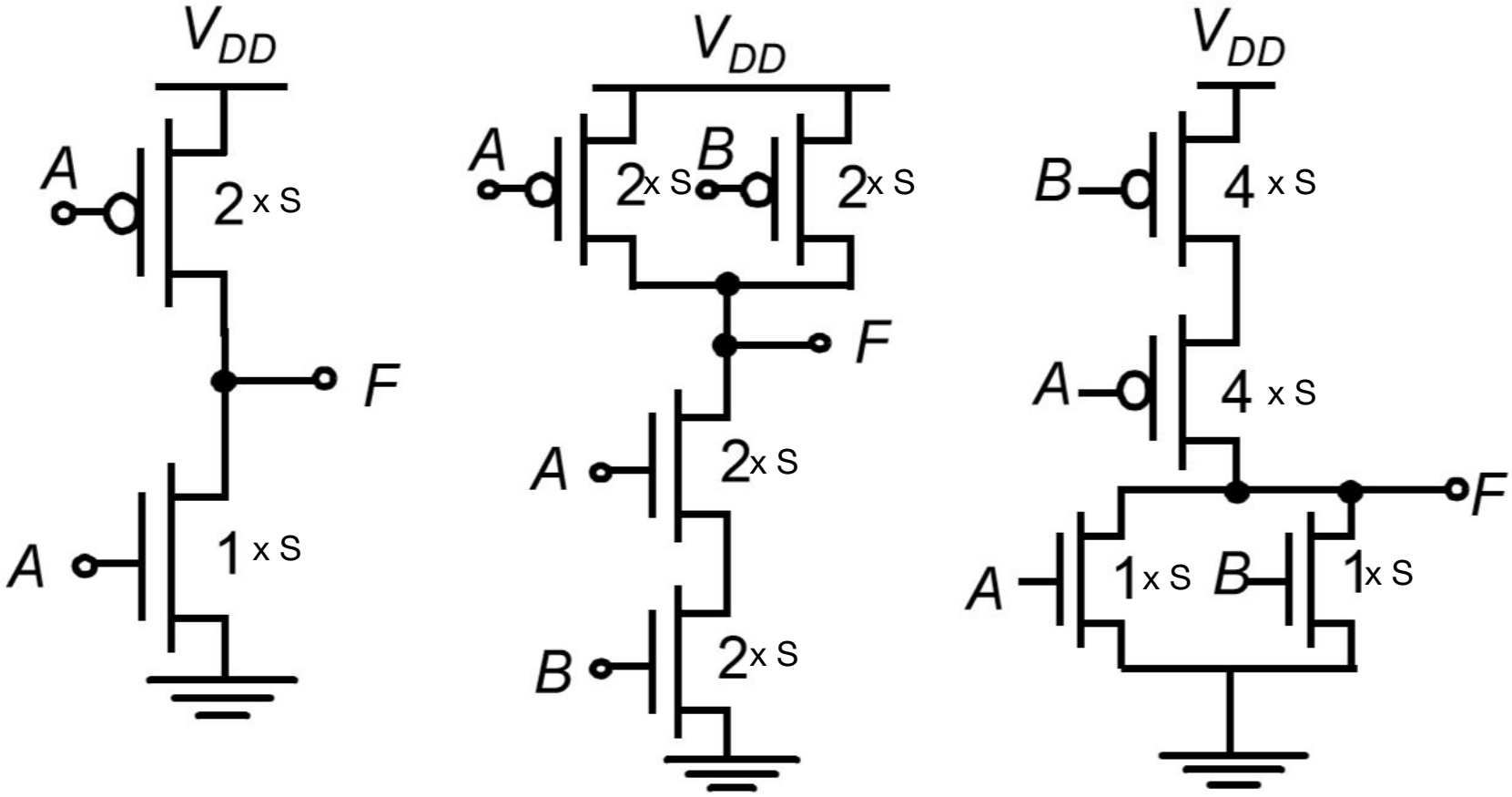
How much self-loading capacitance?





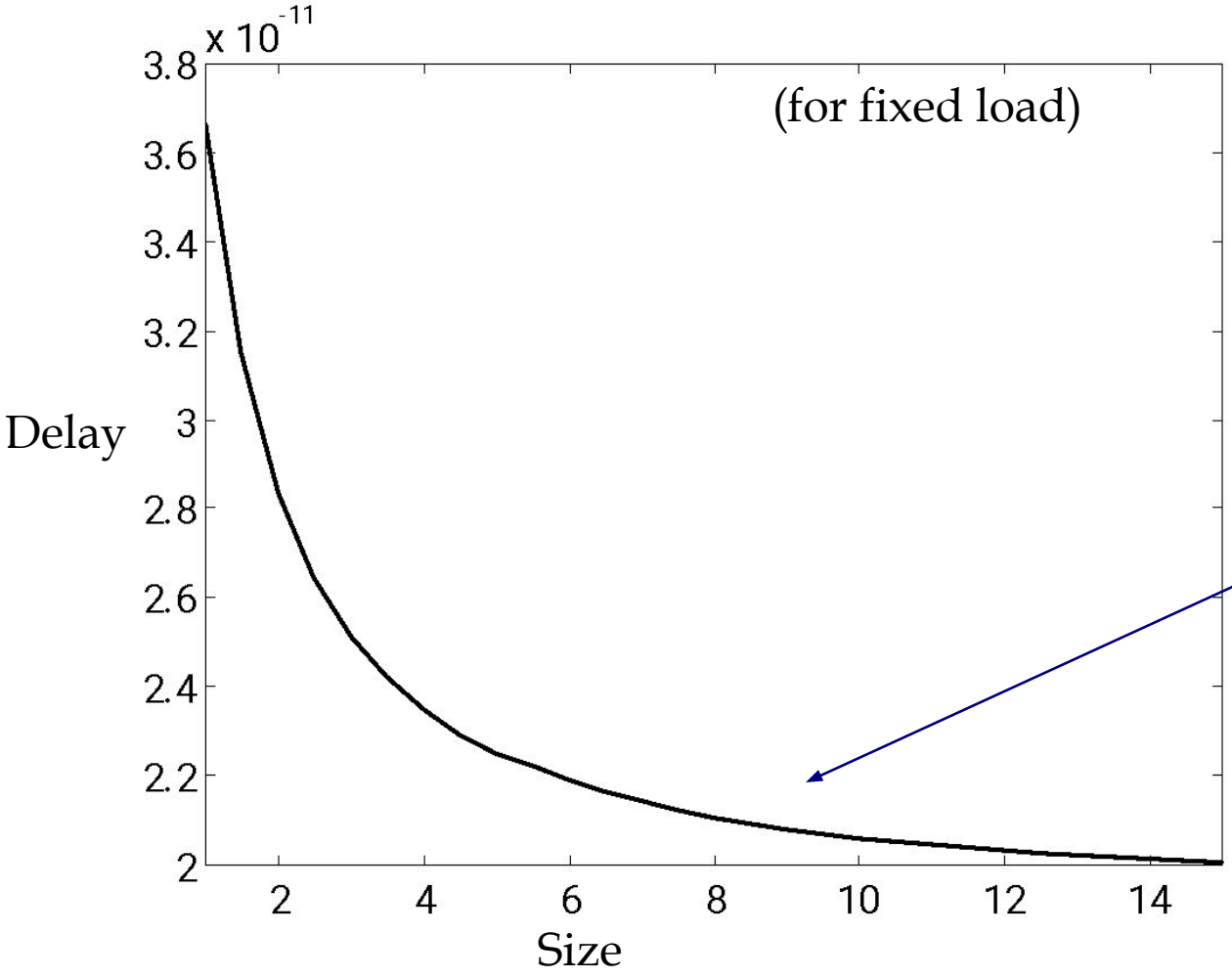
Sizing of Gates

- Relative sizes are preserved
- inv_1, inv_2, inv_4 means S=1, S=2, S=4



Self Loading

Consider a gate driving a fixed output cap.



Self-loading effect:
Intrinsic capacitances dominate

Where does power go in CMOS?

- **Dynamic Power Consumption**

  Charging and Discharging Capacitors

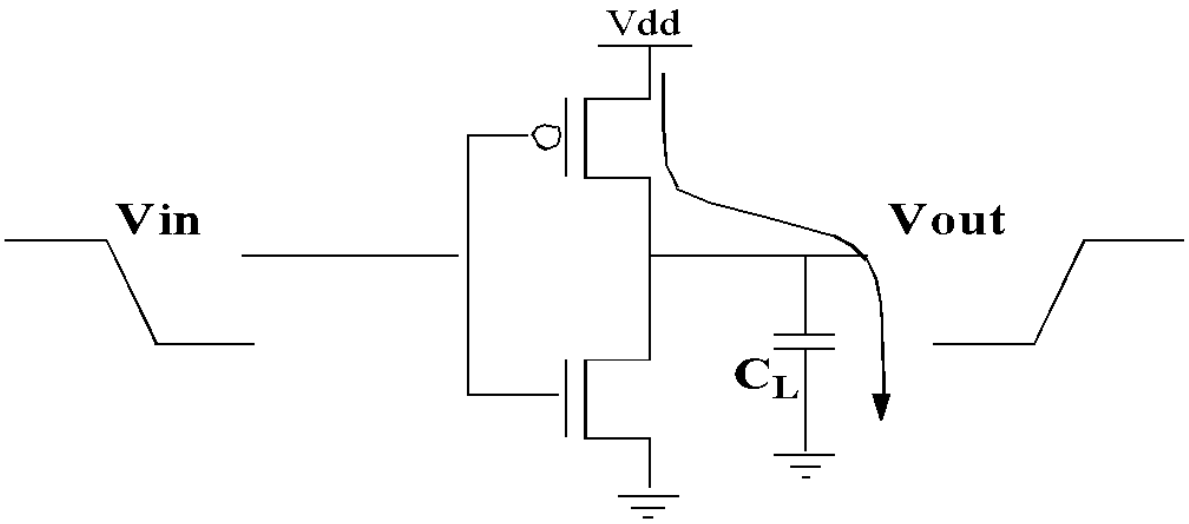
- **Short Circuit Currents**

  Short Circuit Path between Supply Rails during Switching

- **Leakage**

  Leaking diodes and transistors

Power: Dynamic

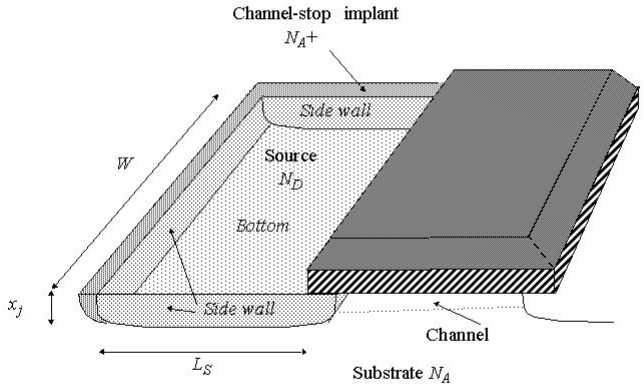


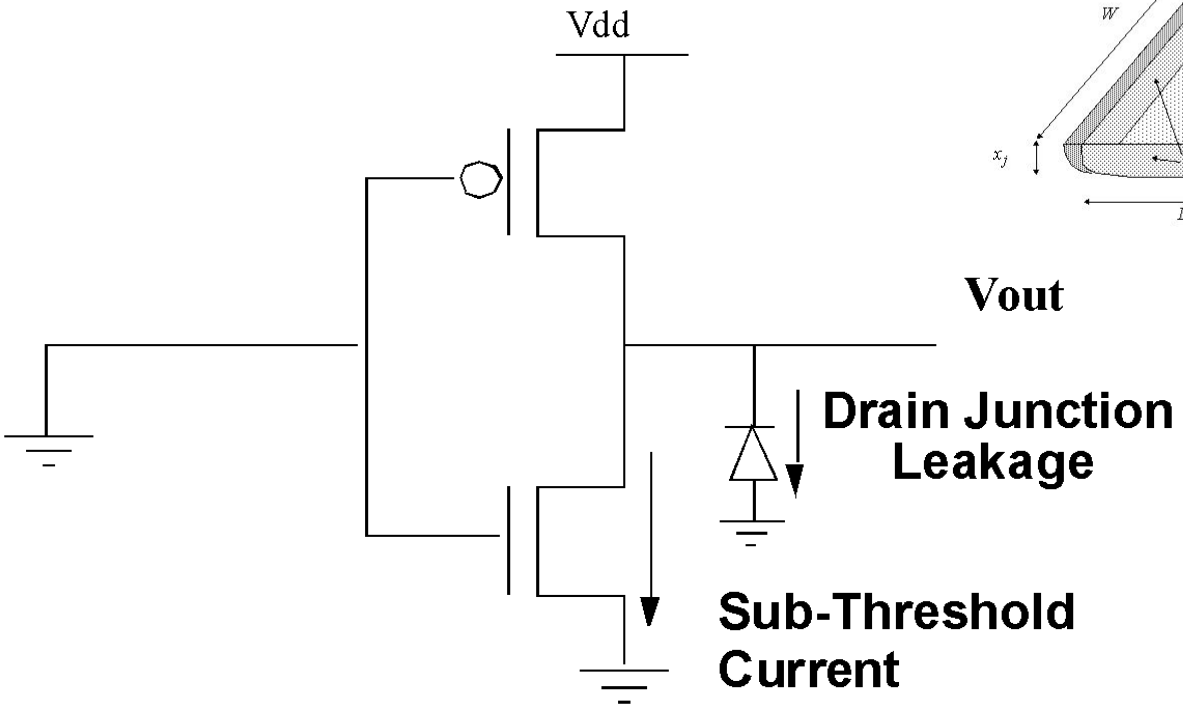
$$\text{Energy/transition} = C_L * V_{dd}^2$$

$$\text{Power} = \text{Energy/transition} * f = C_L * V_{dd}^2 * f$$

- Not a function of transistor sizes!
- Need to reduce C_L, V_{dd}, and f to reduce power.

Power: Leakage

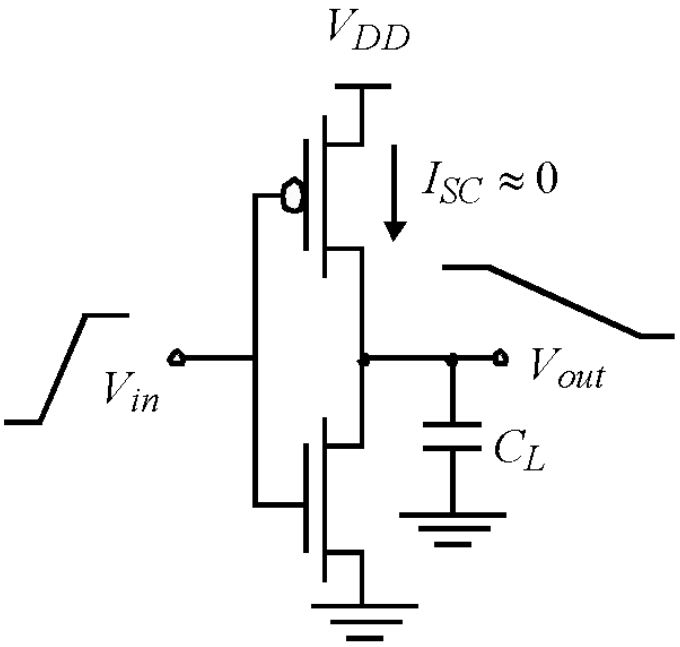




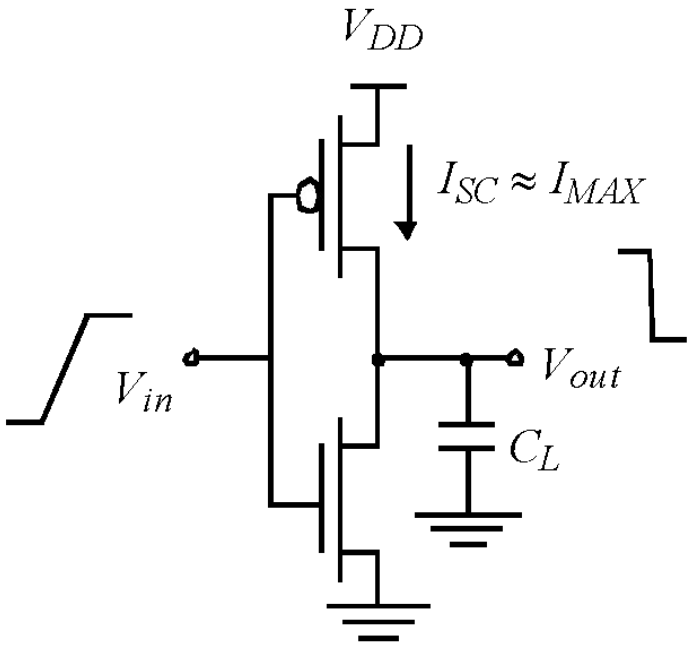
Sub-Threshold Current Dominant Factor

Power: Short Circuit

Both PMOS and NMOS are “on” while a signal is transitioning



Large capacitive load



Small capacitive load

(Some) Low Power Techniques

- Reduce capacitance
  - Use smaller size gates
  - Shorten wires
- Reduce switching
  - Lower frequency
  - Logic gating
- Lower vdd
- Increase Vth (lowers leakage)

Power Reports

OpenLane/designs/picorv32a/runs/CLASS/reports/signoff/31-rcx_sta.power.rpt

```
====================================================================================
 report_power
====================================================================================

======================= Typical Corner ===================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             3.96e-03   1.51e-03   1.35e-08   5.48e-03  25.5%
Combinational          6.79e-03   9.23e-03   5.99e-08   1.60e-02  74.5%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  1.08e-02   1.07e-02   7.33e-08   2.15e-02 100.0%
                          50.0%      50.0%       0.0%
```

Next Lecture

- Interconnect