Lecture 07: OpenLane

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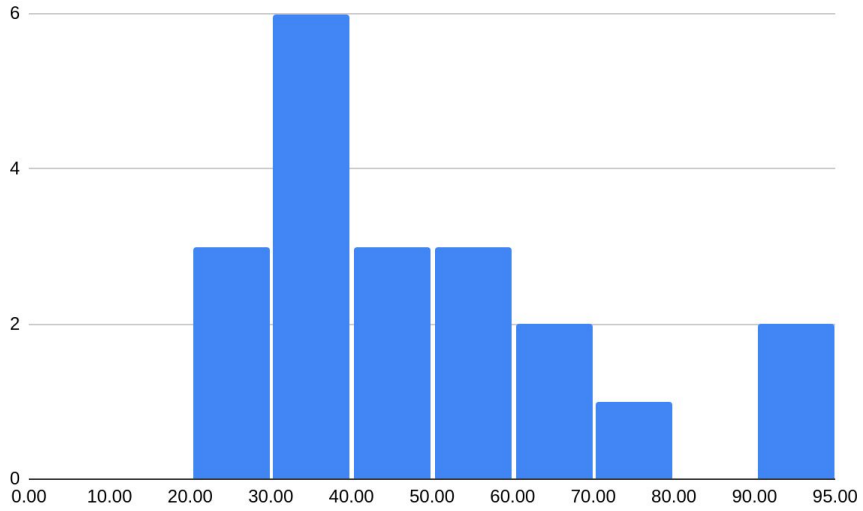
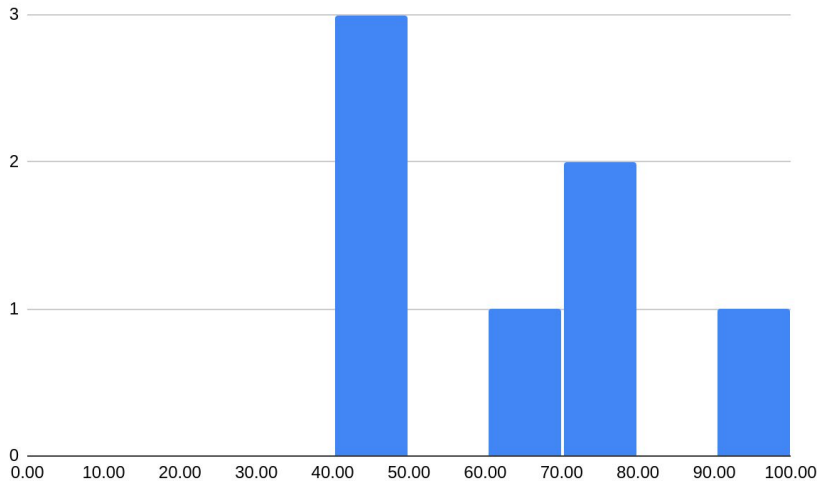
Quiz 1



CSE 122
47% average



CSE 222A
64% average

Partial Credit Quiz 1

Resubmit PDF as quiz1.pdf to git repo.
Will provide blank quiz as well in Slack.

Up to 20% partial credit.

Due this Friday 5pm

HW1 Part 2b Resubmit

We didn't have all the DRC checks enabled! In demo klayout/drc/sky130.lydrc change FEOL from false to true.

```
# enable / disable rule groups
FEOL    = false # front-end-of-line checks
BEOL    = true # back-end-of-line checks
OFFGRID = true # manufacturing grid/angle checks
```

This was why drc4.gds also had an LVS issue. One error wasn't flagged.

Resubmit the GDS by Sunday 4/30 5pm. No penalty. No need to describe additional errors in part 2a.

Today's Lecture

- TCL
- Flow Steps and Control
- Design Directory Structure
- OpenRoad GUI
- Project Configuration
- Design Space Exploration

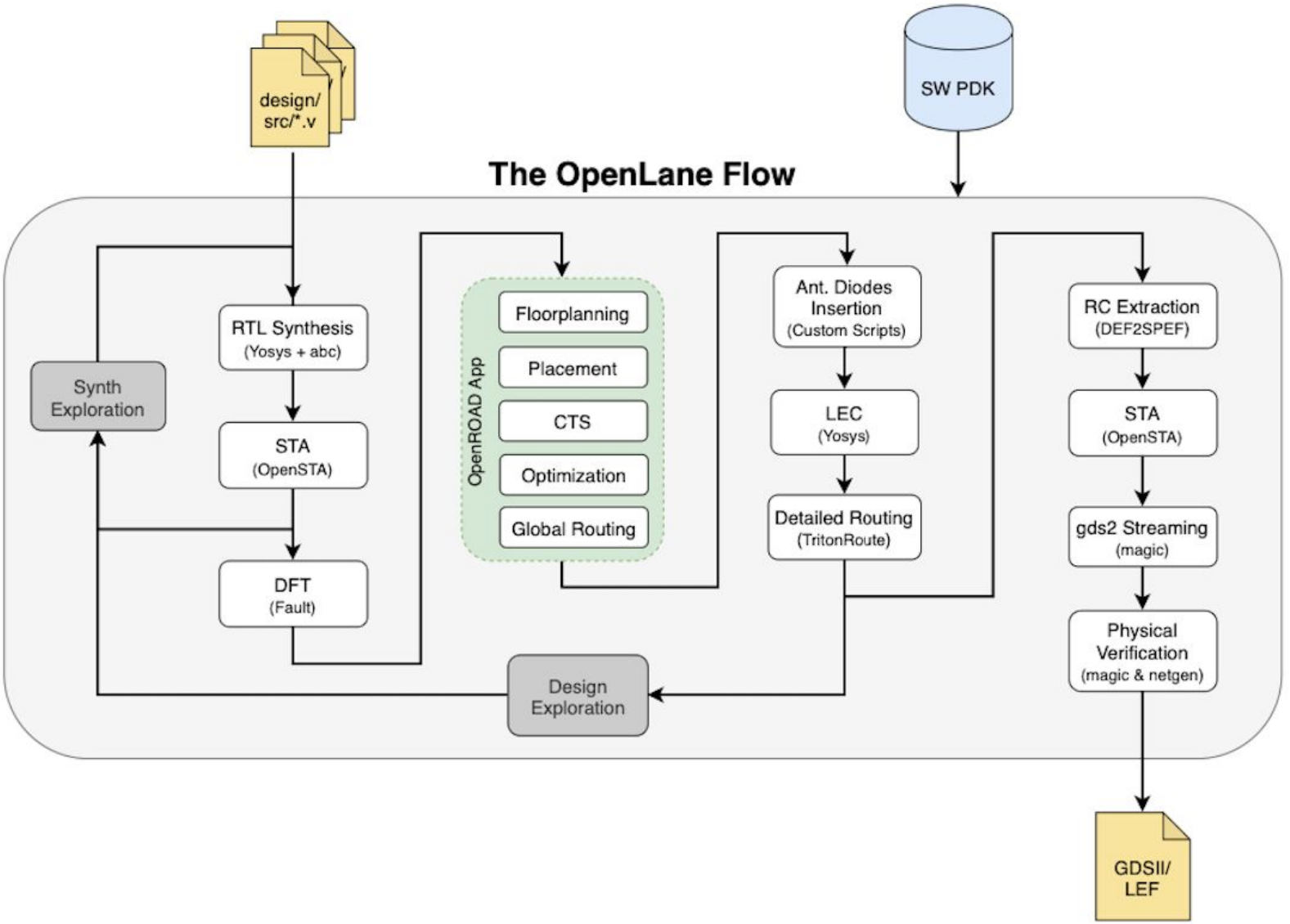
https://openlane.readthedocs.io/

Tool Command Language (TCL)

- https://www.tcl.tk/man/tcl8.5/tutorial/tcltutorial.html
- Scripting (interpreted) language
  - Loops, variables, etc.
  - Regular expressions
- Tool commands are added
  - Links to C, C++, etc. code
- **Used by almost every commercial EDA tool!**

- OpenLane/scripts/tcl_commands
  - OpenLane interface sets up a lot of “defaults” in the technology
  - Examples: init_floorplan, place_io, run_sta, etc.
- OpenLane/scripts/openroad
  - OpenRoad provides commands for different tools
  - clock_tree_synthesis, detailed_placement

Flow Steps


design/
src/*.v
SW PDK
The OpenLane Flow
Synth
Exploration
RTL Synthesis
(Yosys + abc)
STA
(OpenSTA)
DFT
(Fault)
OpenROAD App
Floorplanning
Placement
CTS
Optimization
Global Routing
Ant. Diodes
Insertion
(Custom Scripts)
LEC
(Yosys)
Detailed Routing
(TritonRoute)
RC Extraction
(DEF2SPEF)
STA
(OpenSTA)
gds2 Streaming
(magic)
Physical
Verification
(magic & netgen)
Design
Exploration
GDSII/
LEF

Flow Control

flow.tcl

Arguments:
-design

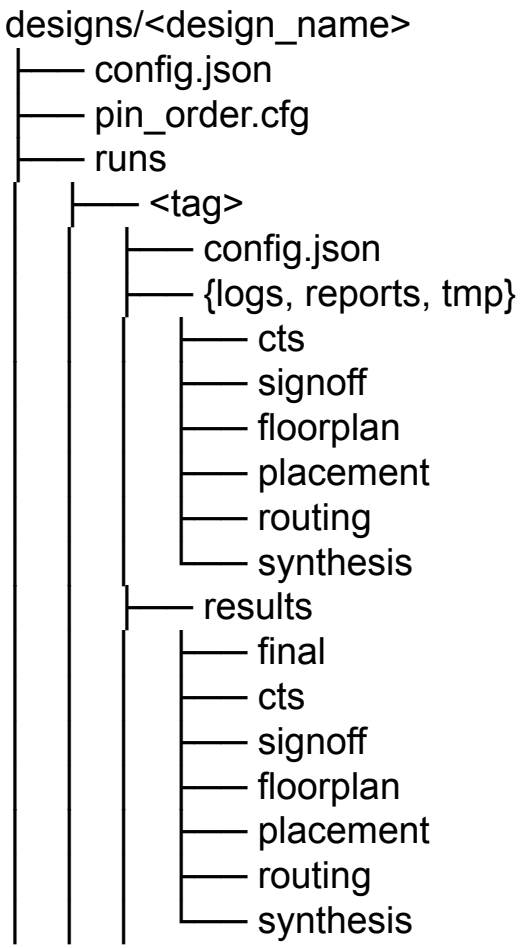
-from
-to

-tag

-overwrite

```
set steps [dict create \
    "synthesis" "run_synthesis" \
    "floorplan" "run_floorplan" \
    "placement" "run_placement_step" \
    "cts" "run_cts_step" \
    "routing" "run_routing_step" \
    "parasitics_sta" "run_parasitics_sta_step" \
    "eco" "run_eco_step" \
    "diode_insertion" "run_diode_insertion_2_5_step" \
    "irdrop" "run_irdrop_report_step" \
    "gds_magic" "run_magic_step" \
    "gds_klayout" "run_klayout_step" \
    "lvs" "run_lvs_step $LVS_ENABLED " \
    "drc" "run_drc_step $DRC_ENABLED " \
    "antenna_check" "run_antenna_check_step $ANTENNACHECK_ENABLED " \
    "cvc_rv" "run_erc_step"
]
```

Design Directory Structure



- Each design has a config.tcl (older) or config.json (preferred)
- Optional pin placement file
- Optional SDC (Synopsys Design Constraints) file

Synthesis

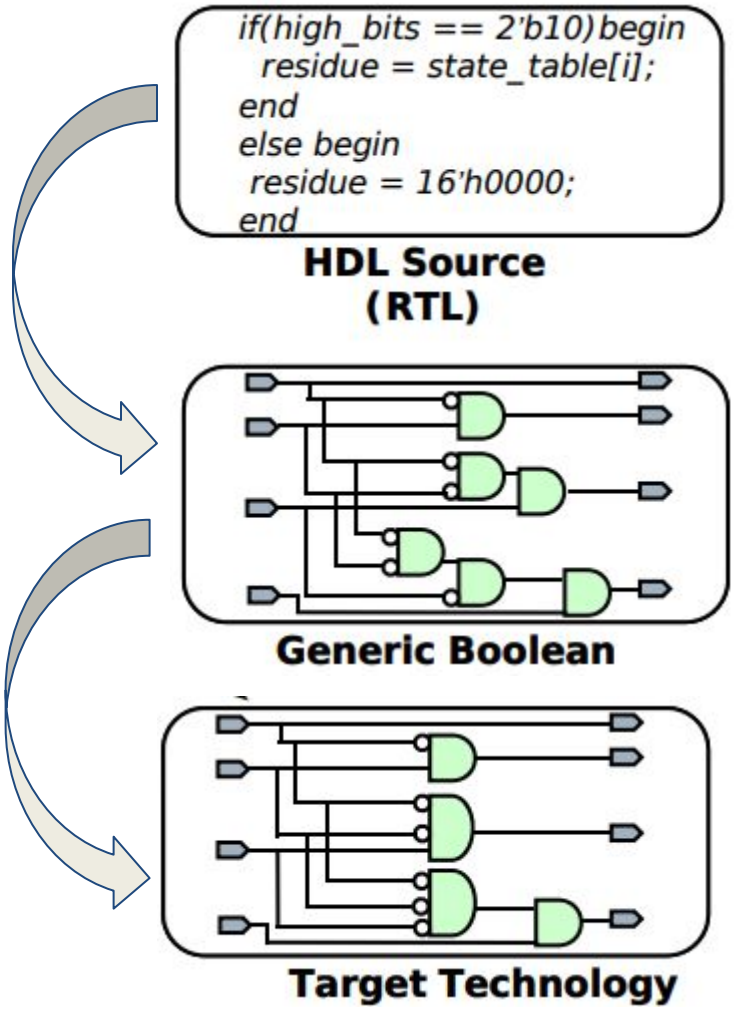
Goal: Map Verilog to gate-level netlist

Two stages:

1) Logic Minimization
2) Technology Mapping

Metrics:

Number of gates
Size of gates
Delay/Power

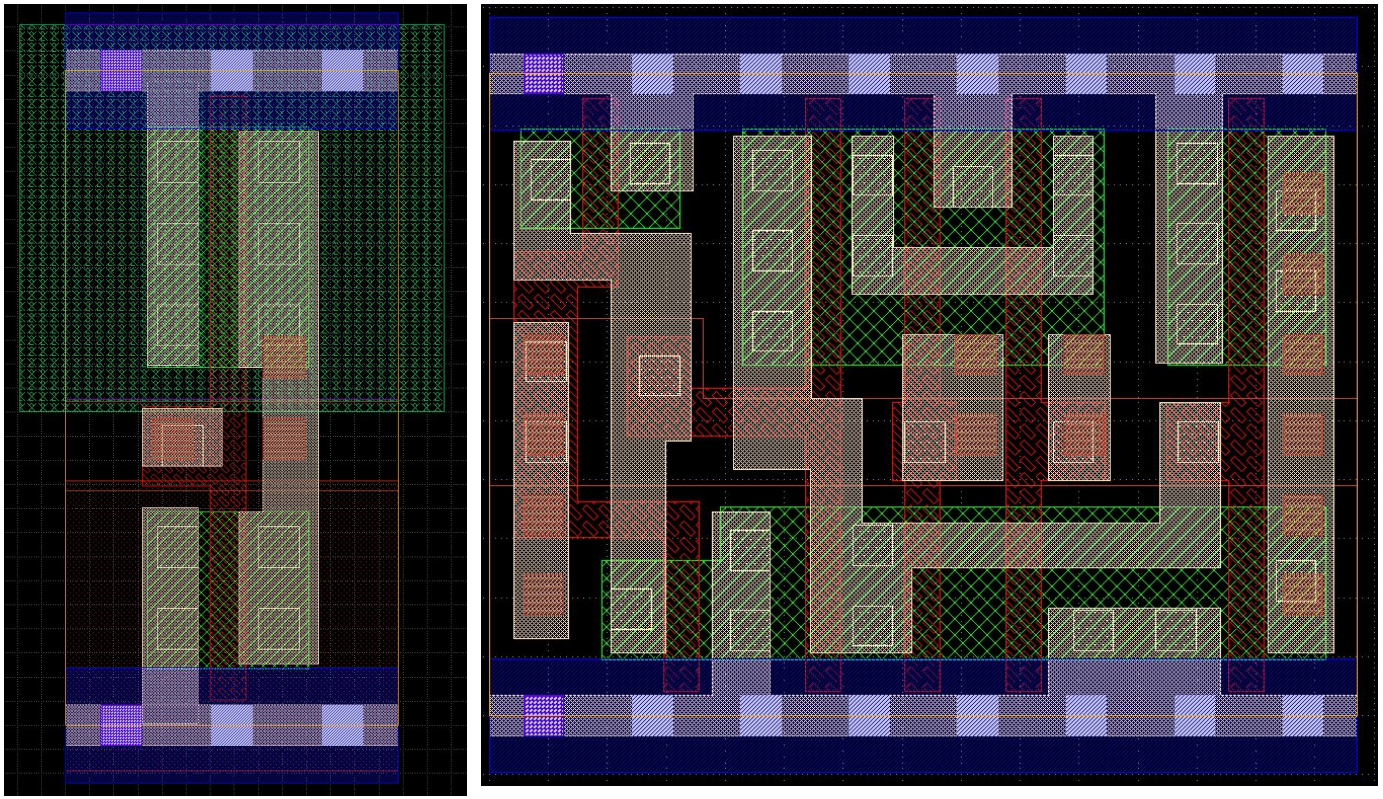


Standard Cell Libraries

Fixed height cells

Different logic functions (nand, mux, aoi221)

Sequential cells (flip-flops and latches)

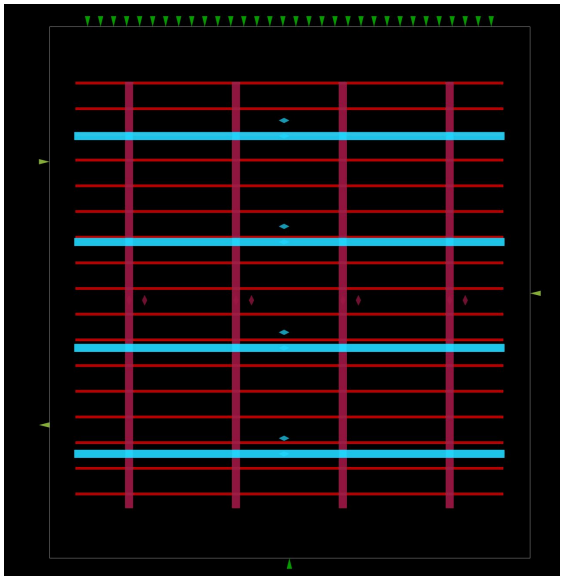


Floorplan

Goal: Create the high-level chip/block plan

Stages:

1) Determine chip/block area
2) IO placement
3) Block placement
4) Define standard cell rows
5) Power planning



Metrics:

Area

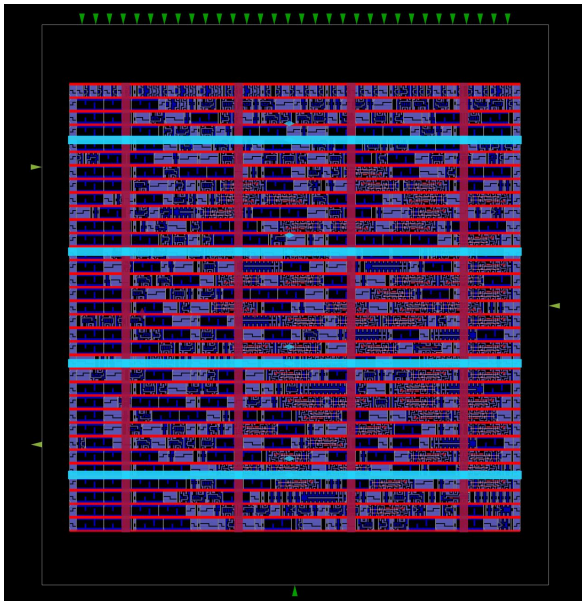
Area utilization

Placement

Goal: Determine locations of all logic gates

Stages:

1) Global Placement
2) Detailed Placement



Metrics:

Minimize wire length

Minimize congestion

Minimize timing

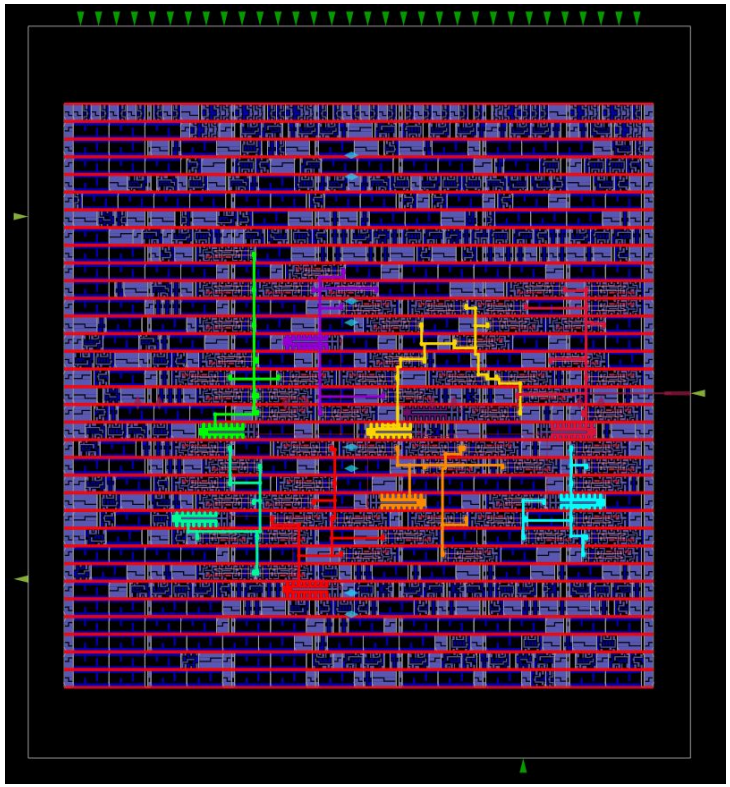
CTS

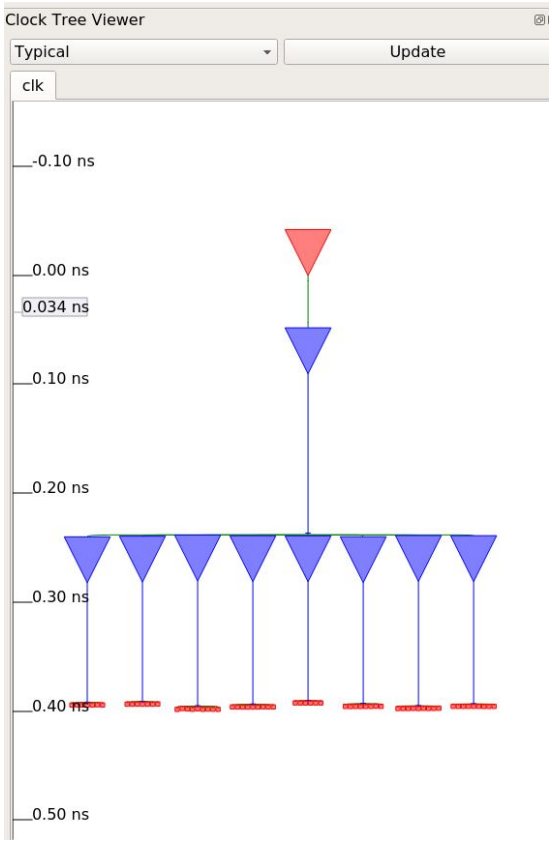
Goal: Determine clock buffer and wire locations

Metrics:

Skew

Power





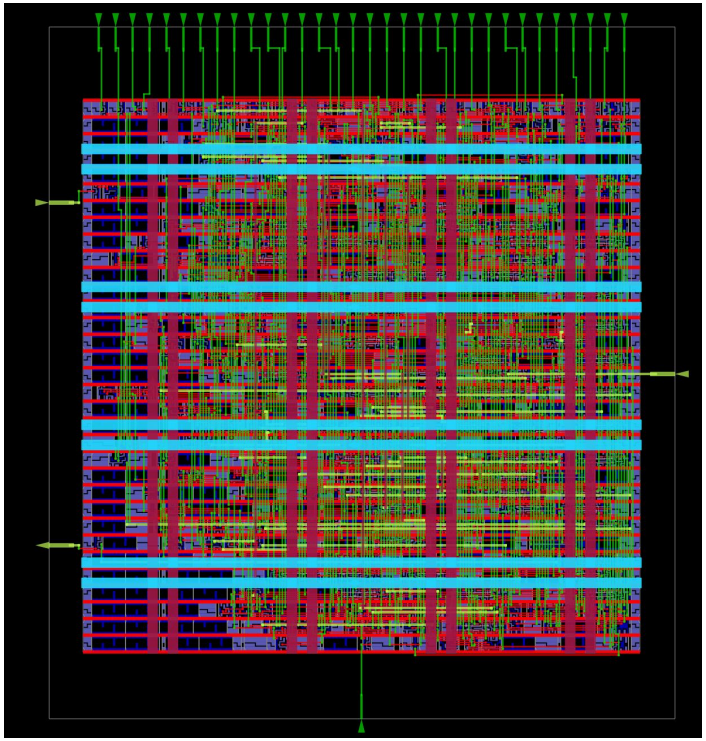
Routing

Goal: Connect all signals on gates using multiple metal layers

Two stages:

1) Global Routing
2) Detailed Routing

Metrics:
Wire length
Congestion
Delay
Power



Static Timing Analysis (STA)

Goal: Evaluate timing (and power) of circuit

Evaluates minimum and maximum (hold and setup) times of all paths
Static means it doesn't consider logic function
Ideal or non-ideal clocks
Run at each stage of design

Metrics:
Delay
Slack
Dynamic power
Leakage power

Remaining Steps

Parasitics STA

Engineering Change Order (ECO)

Diode Insertion

IR Drop

GDS Generation

Layout vs. Schematic (LVS)

Design Rule Check (DRC)

Antenna Check

Circuit Validity Checks (CVC)

Project Discussion

Project Consult

Informal discussion with Jesse and/or I before you write a proposal. Due in 1 week.

Project Proposal

1-2 page proposal. Due in 2 weeks.

Demo!

Example TCL Scripts

Example config.json

Viewing reports and results

Using OpenRoad GUI

Next Lecture

- Cell libraries
- Next next lecture: Static Timing Analysis