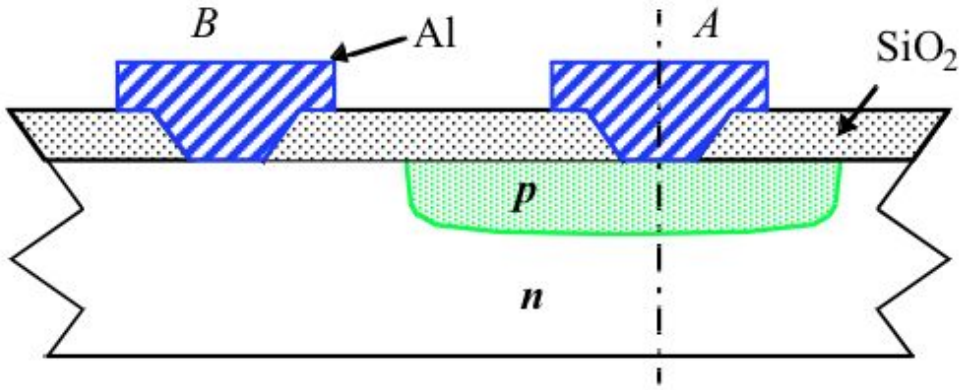
Lecture 04: Devices and CMOS

Matthew Guthaus
Professor
UCSC, Computer Science & Engineering
http://vlsida.soe.ucsc.edu
mrg@ucsc.edu

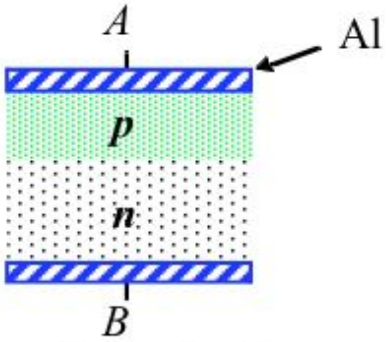
Today's Lecture

- Semiconductor Devices
  - Diode
  - Field Effect Transistor (FET)
  - Width, Length and R_{on}
  - Body Connection
  - Parasitic Capacitance and Resistance
- CMOS Review

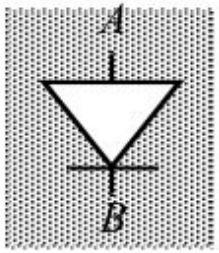
The Diode



Cross-section of *pn*-junction in an IC process



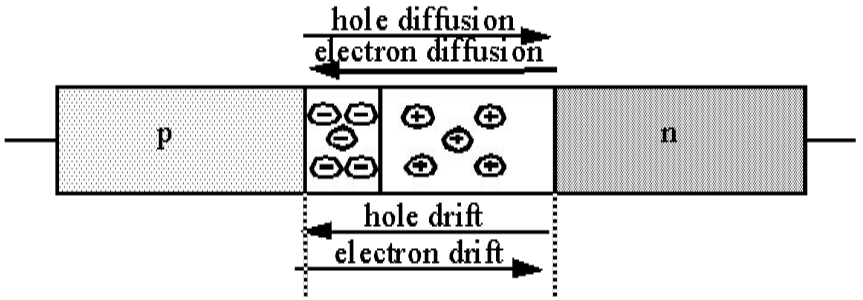
One-dimensional representation



diode symbol

3

Depletion Region



(a) Current flow.

$$\phi_t = \frac{k \cdot T}{q}$$

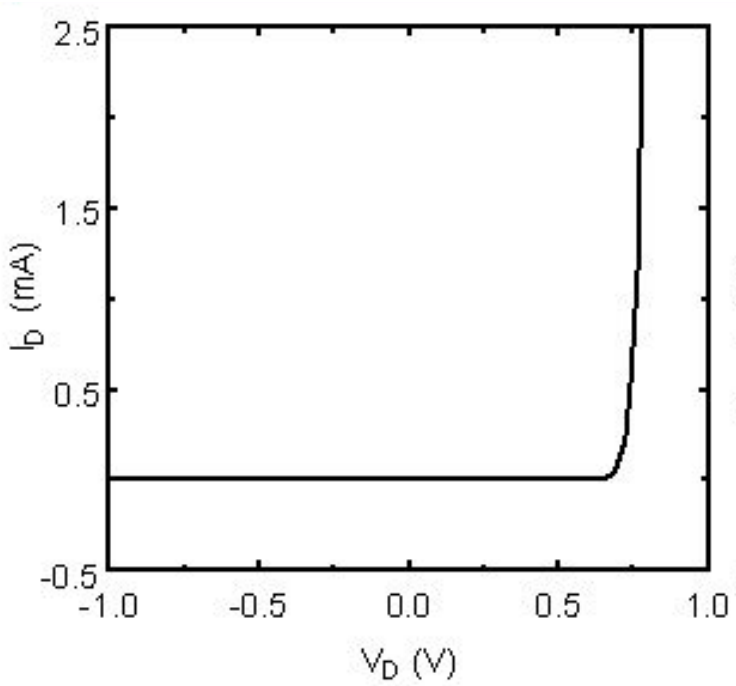
$$\phi_0 = \phi_T \ln\left[\frac{N_A N_D}{n_i^2}\right]$$

Drift is charge based
Diffusion is concentration based

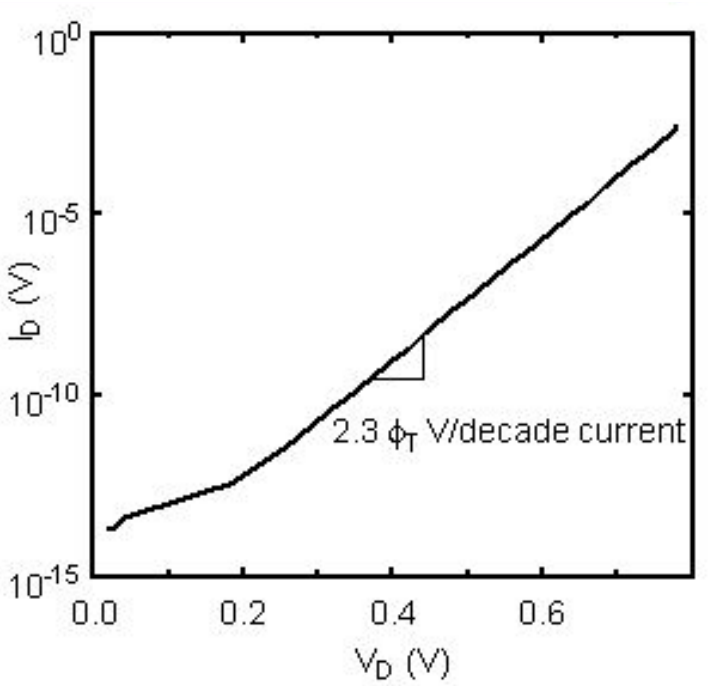
N_A is concentration of acceptors
N_D is concentration of donors
n_i is "intrinsic concentration"

$$\phi_0 = 26 \ln\left[\frac{10^{15} \times 10^{16}}{2.25 \times 10^{20}}\right] \text{mV} = 638 \text{ mV}$$

Diode Current



(a) On a linear scale.

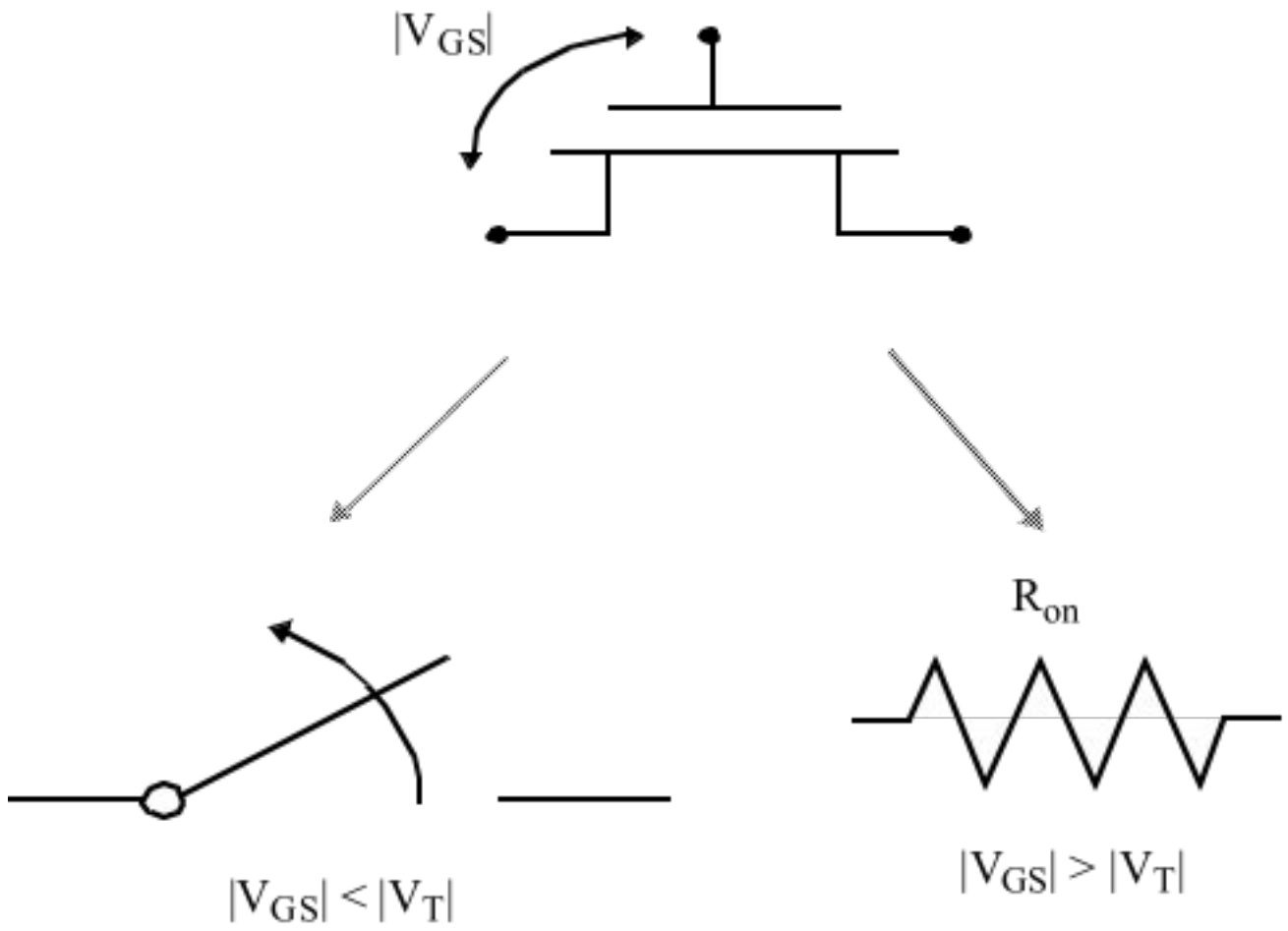


(b) On a logarithmic scale (forward bias).

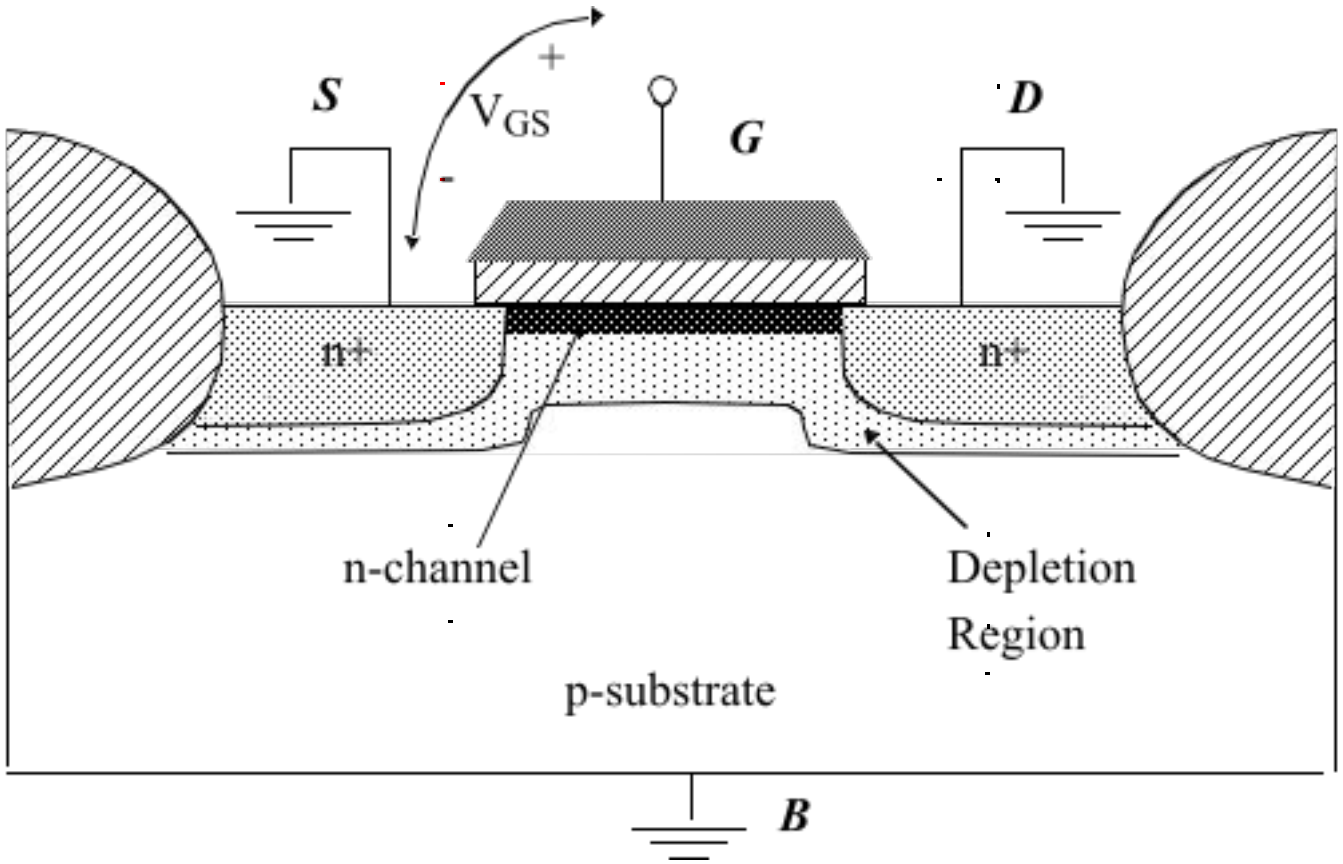
$$I_D = I_S\left(e^{V_D/\phi_T} - 1\right)$$

$$\phi_t = \frac{k \cdot T}{q}$$

Switch Model of CMOS Transistor



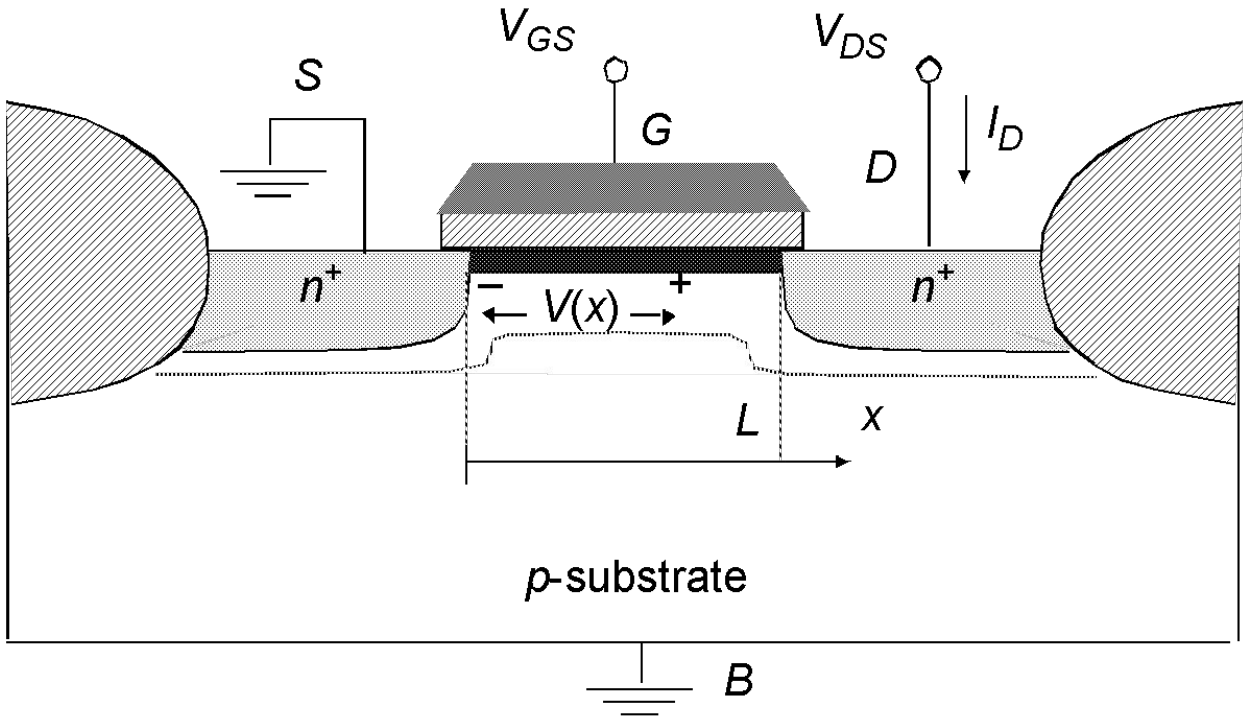
Threshold Voltage: Concept



7

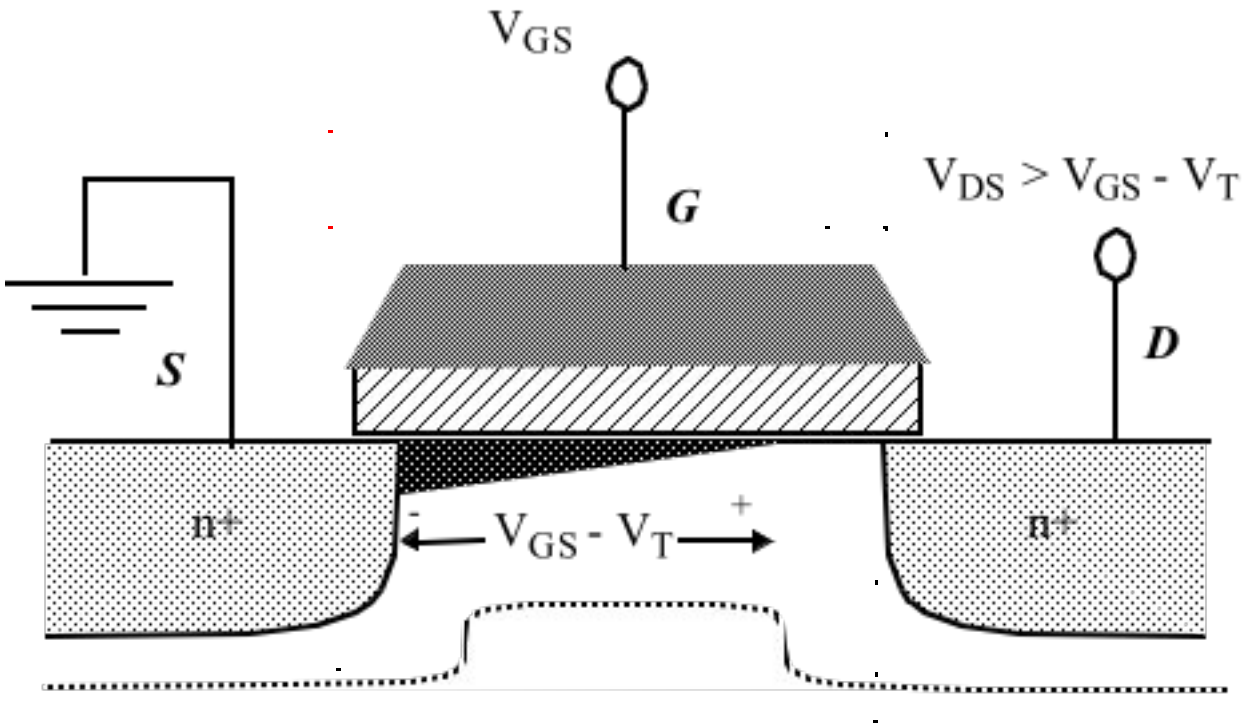
Transistor in Linear

If you use a voltage across the "resistor" within a range, it behaves like a resistor: Vds < Vgs - Vth



MOS transistor and its bias conditions

Transistor in Saturation



Current-Voltage Relations

Linear Region: $V_{DS} \leq V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

with

$$k'_n = \mu_n C_{ox} = \frac{\mu_n \varepsilon_{ox}}{t_{ox}}$$

Process Transconductance Parameter

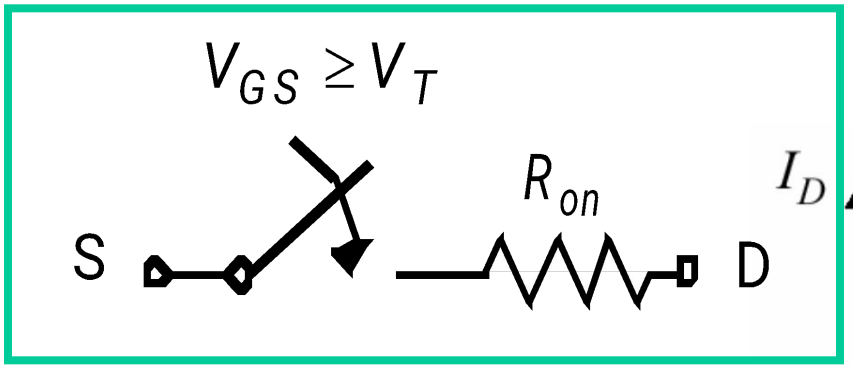
Saturation Mode: $V_{DS} \geq V_{GS} - V_T$

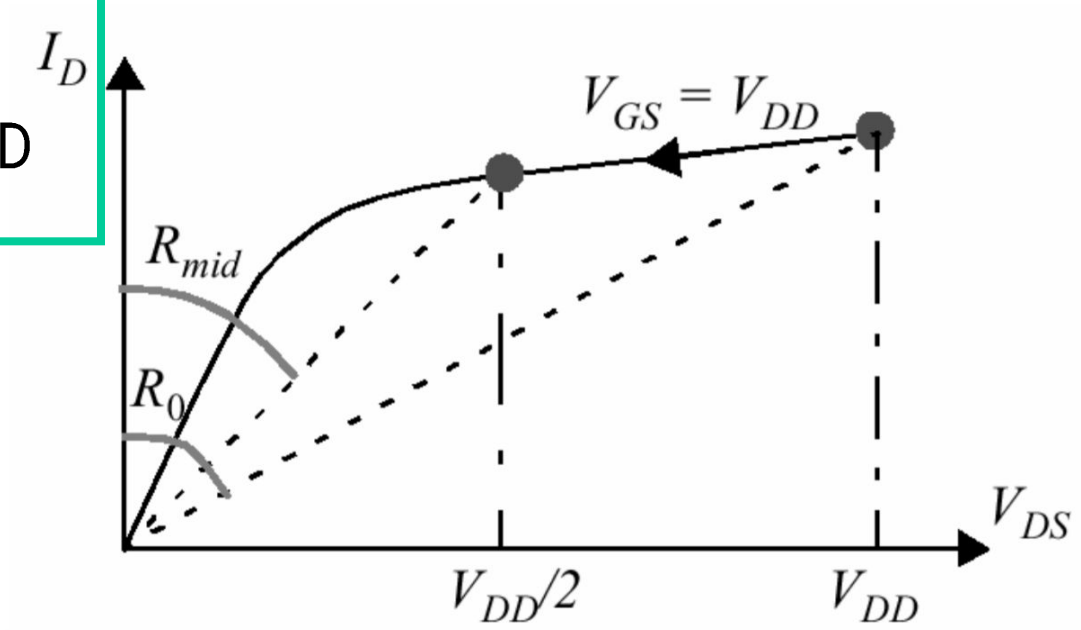
Channel Length Modulation

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

Mobility of electrons is ~2-3x that of holes.

Transistor as a Switch





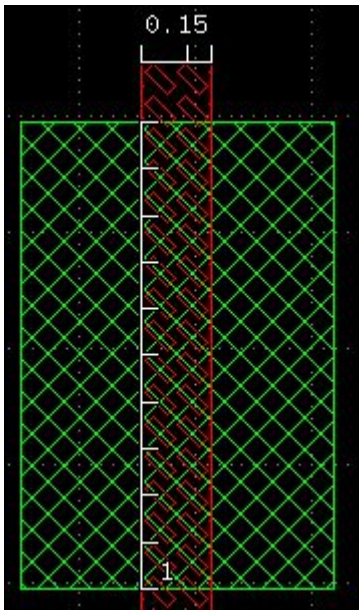
Resistors should be linear, right?

R = Vds / Id
Ron ≅ average(R0, Rmid)

Width, Length, and Ron

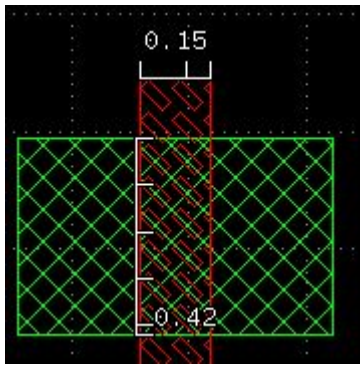
$$I_D = k'_n \frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right)$$

$$I_D = \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$



W

L

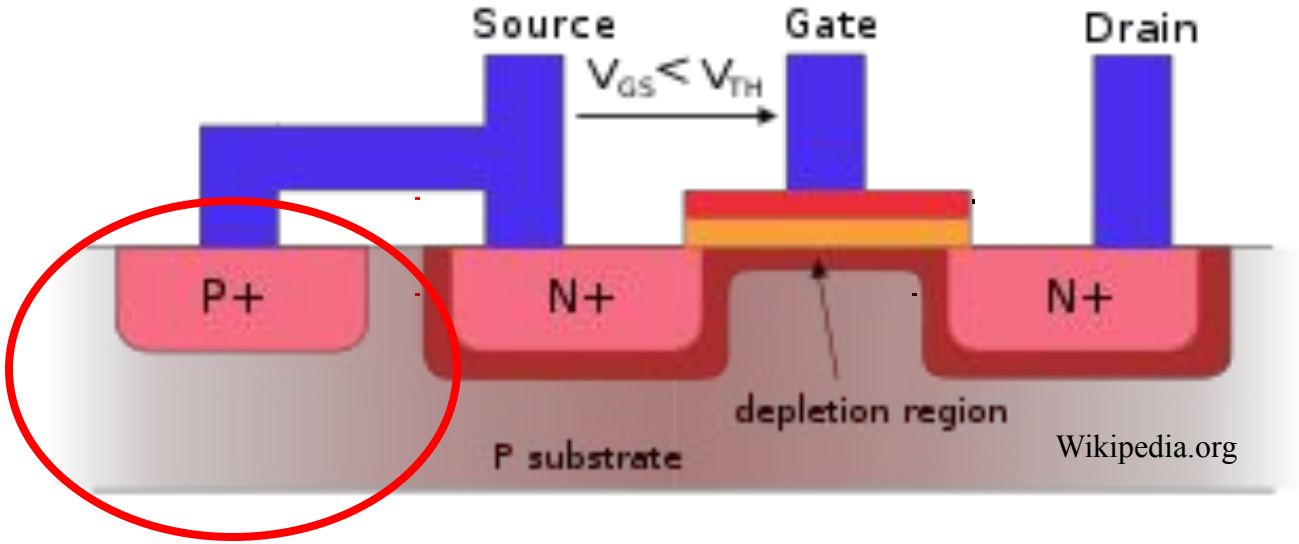


W

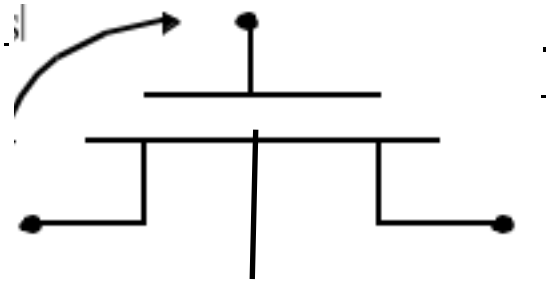
L

Ron ∝ Vds / Id
Id ∝ W / L
Ron ∝ (Vds * L) / W

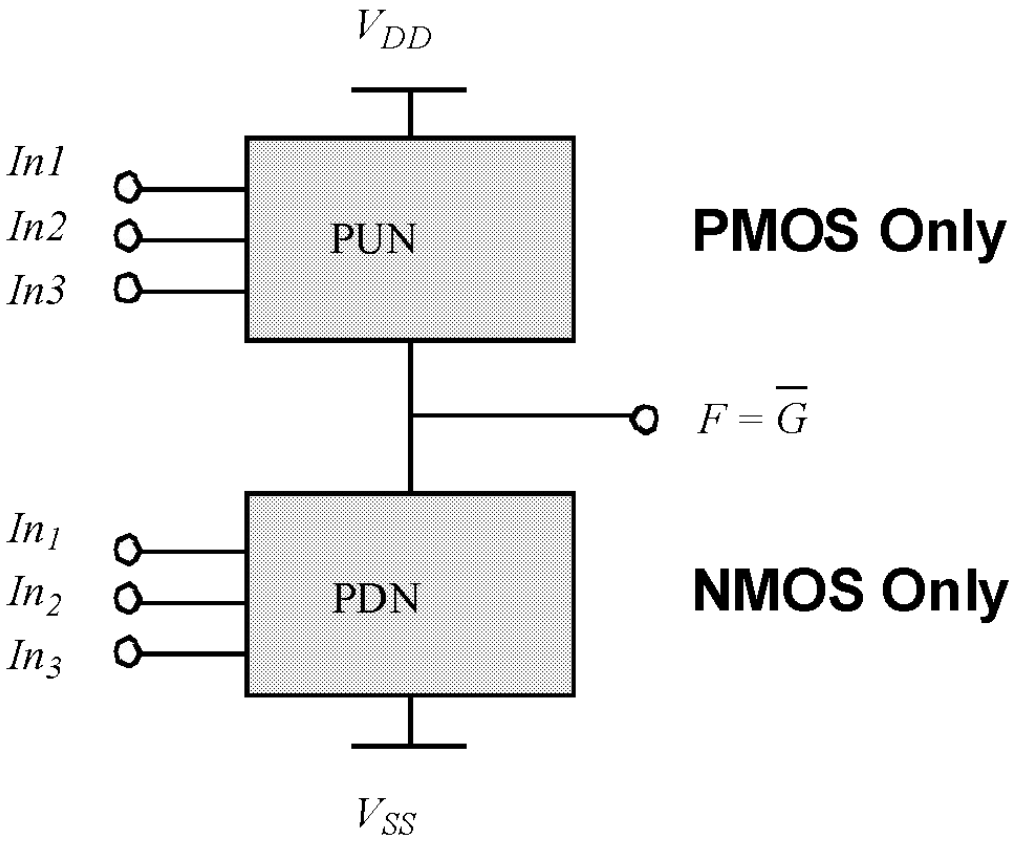
Back-Gate Biasing



If a pwell or nwell (or bulk), can bias the well to adjust threshold.



Static CMOS

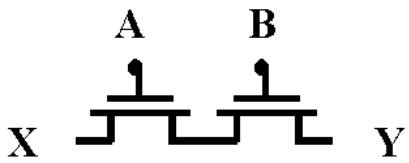


PUN and PDN are Dual Networks

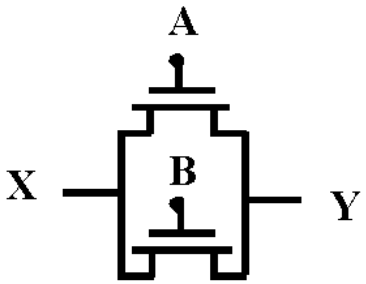
NMOS Transistors in Series/Parallel Connection

Transistors can be thought as a switch controlled by its gate signal

NMOS switch closes when switch control input is high



Y = X if A and B

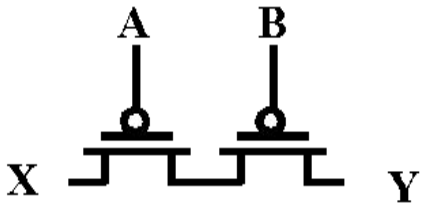


Y = X if A OR B

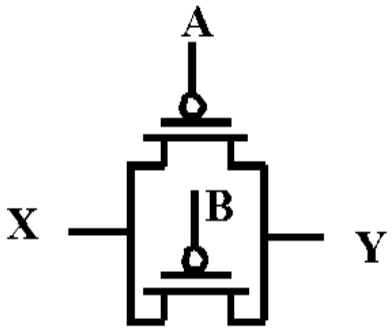
NMOS Transistors pass a "strong" 0 but a "weak" 1

PMOS Transistors in Series/Parallel Connection

PMOS switch closes when switch control input is low



$Y = X$ if $\overline{A}$ AND $\overline{B} = \overline{A + B}$



$Y = X$ if $\overline{A}$ OR $\overline{B} = \overline{AB}$

PMOS Transistors pass a "strong" 1 but a "weak" 0

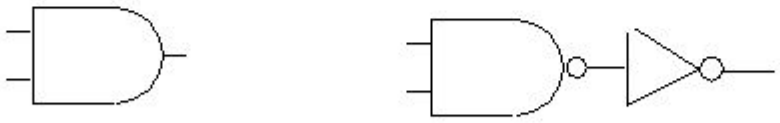
Complementary CMOS Logic Style Construction (cont.)

- **PUP is the DUAL of PDN**
  (can be shown using DeMorgan's Theorem's)

$$\overline{A + B} = \bar{A}\bar{B}$$

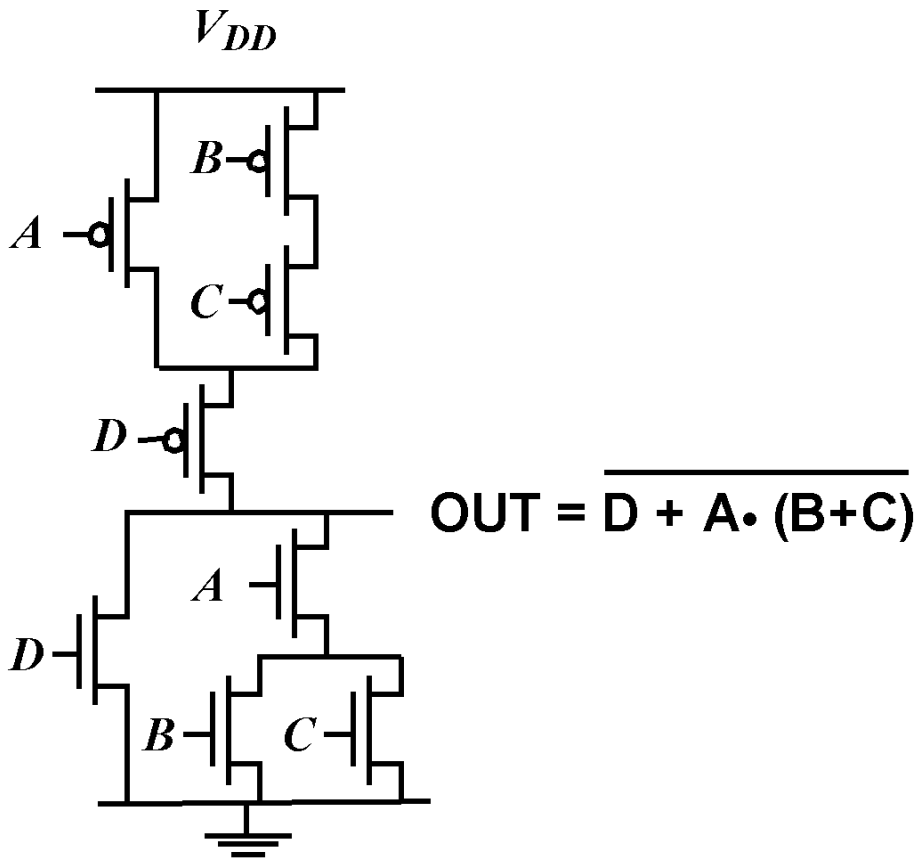
$$\overline{AB} = \bar{A} + \bar{B}$$

- **The complementary gate is inverting**

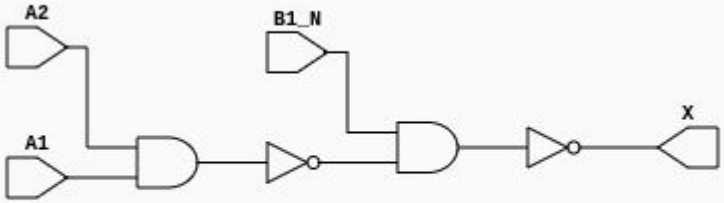


AND = NAND + INV

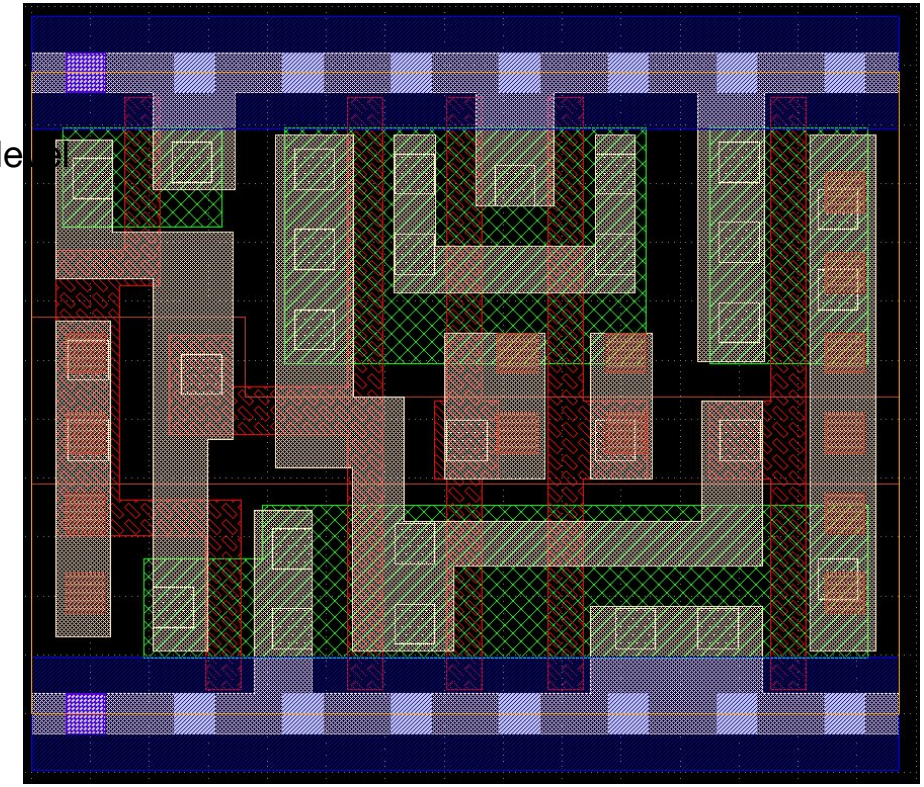
Example Gate: COMPLEX CMOS GATE



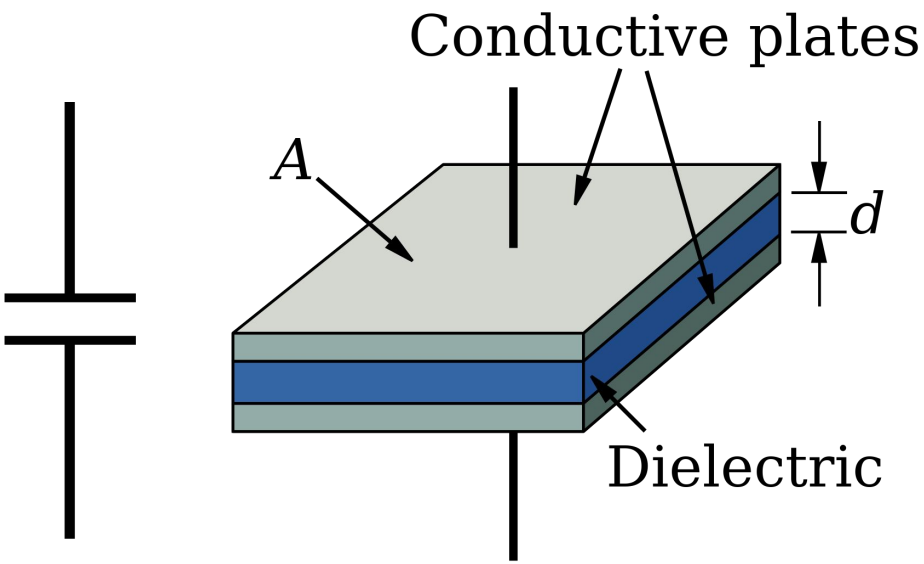
Example: Sky130 a21bo Gate

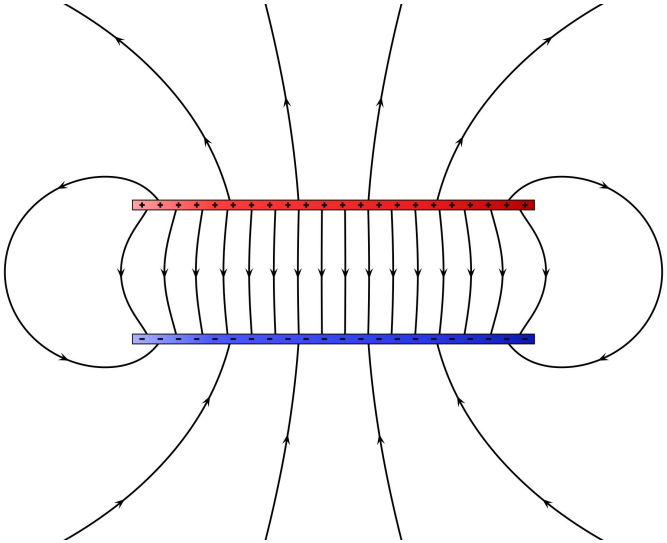


(NOTE: This is the logical schematic, not a transistor le[illegible] schematic!)



Parallel Plate Capacitance



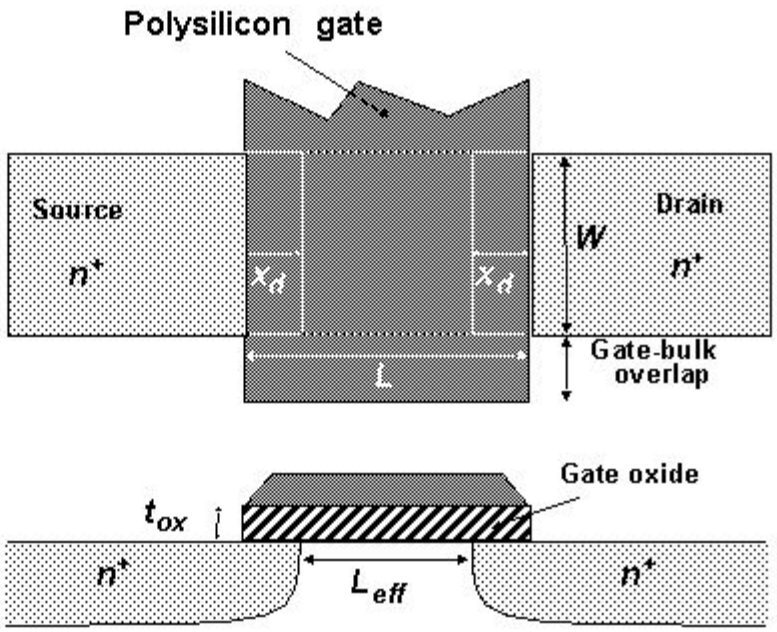


$C = \varepsilon A / d$

The Gate Capacitance

(a) Top view.

(b) Cross-section



$$C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} WL$$

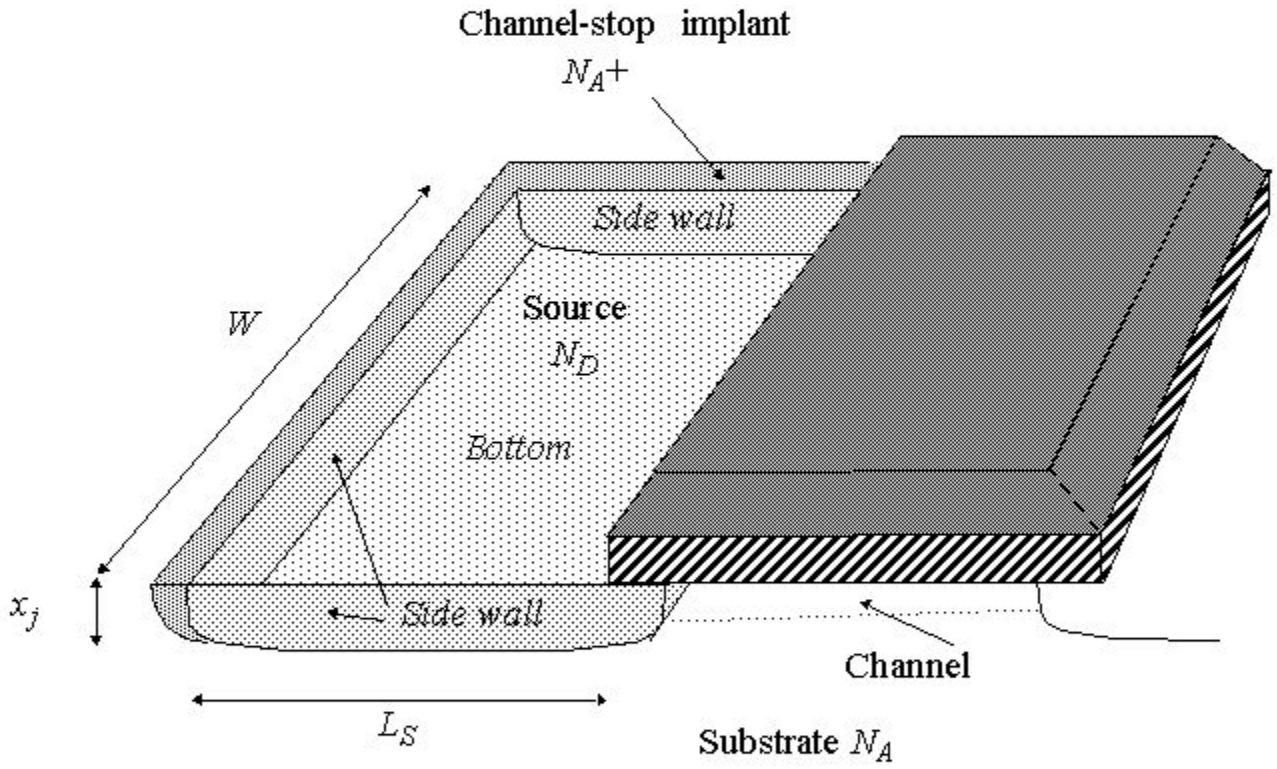
C= εA / d

A = WL

$d = t_{ox}$

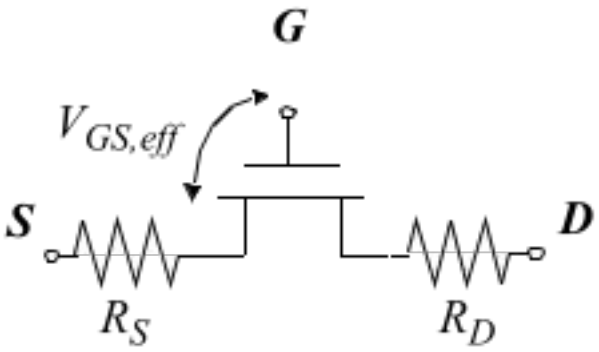
$\varepsilon = \varepsilon_{ox}$

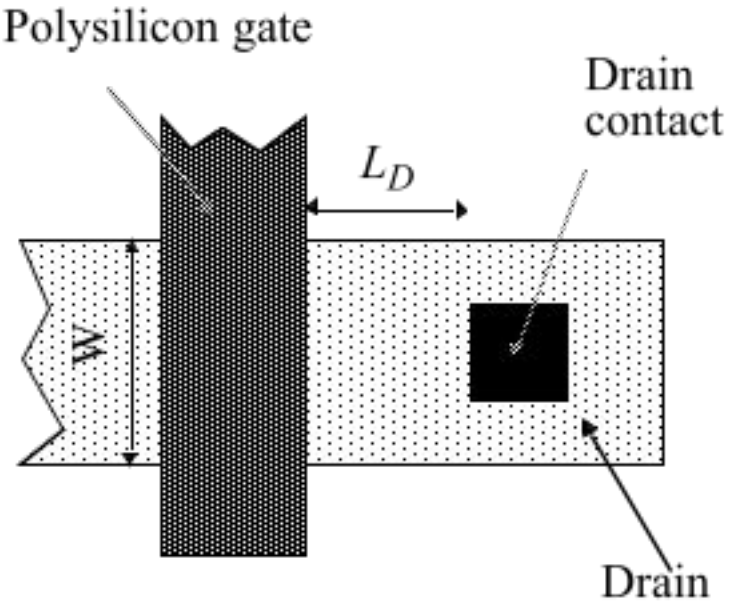
Diffusion Capacitance



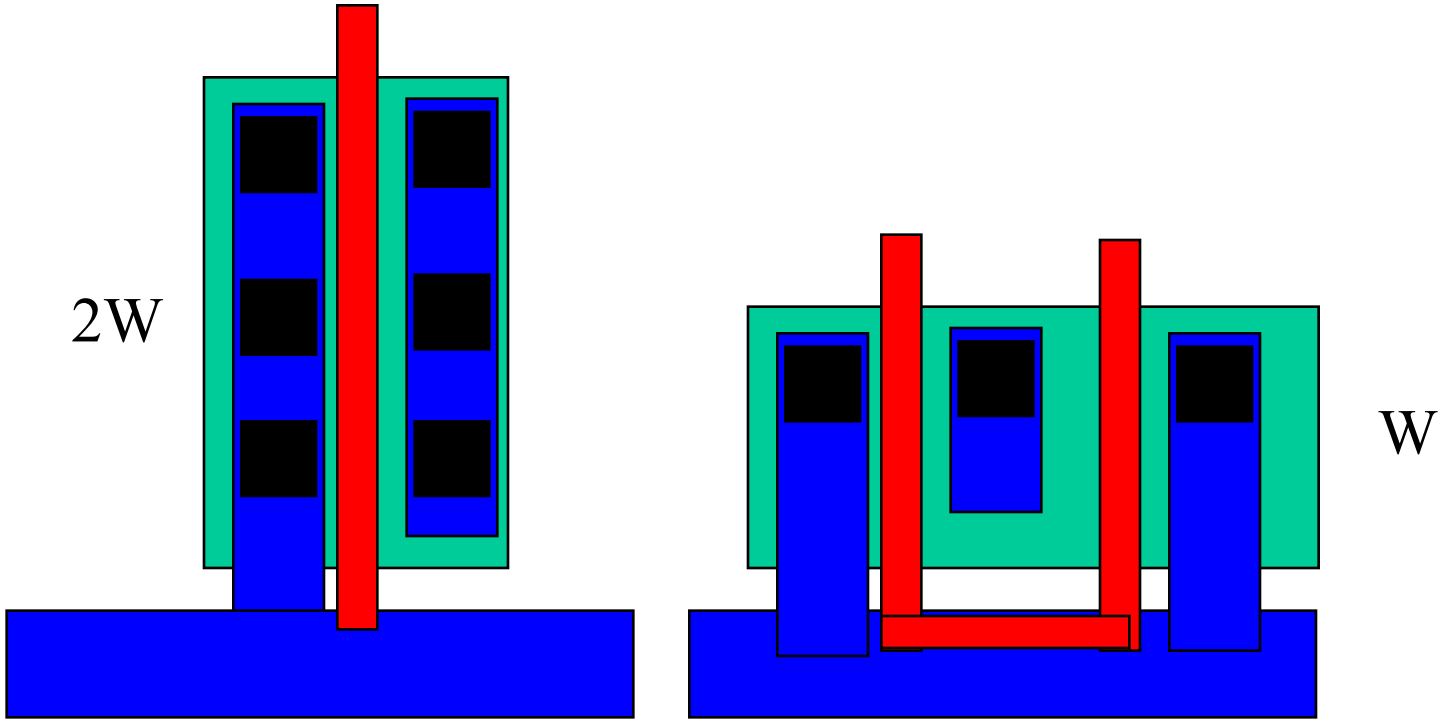
$$C_{diff} = C_{bottom} + C_{sw} = C_j \times AREA + C_{jsw} \times PERIMETER$$
$$= C_j L_S W + C_{jsw}(2L_S + W)$$

Parasitic Resistances





Folding Transistors



Next Class

- Tuesday: Jesse lecture
  - Help with klayout
  - OpenRAM memory generation
  - Review Q&A
- Thursday: Quiz 1