Lecture 03: Layout

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Today's Lecture

- Layers and Masks
- Design Rules
- Transistor Layout
- Klayout and DRC/LVS demo!

Design Rules

- Interface between the circuit designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum feature size (transistor gate length)
  - scalable design rules: lambda parameter
  - absolute dimensions: micron rules
- Rules constructed to ensure that design works even when small fab errors (within some tolerance) occur
- A complete set includes
  - set of layers
  - intra-layer: relations between objects in the same layer
  - inter-layer: relations between objects on different layers

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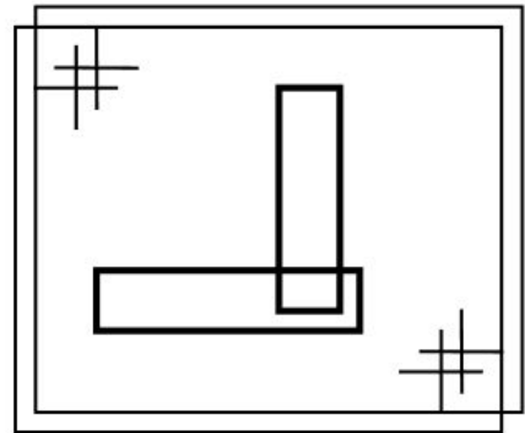
Why Have Design Rules?

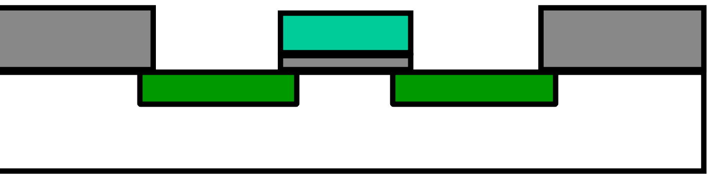
To be able to tolerate some level of fabrication errors such as

1. Mask misalignment



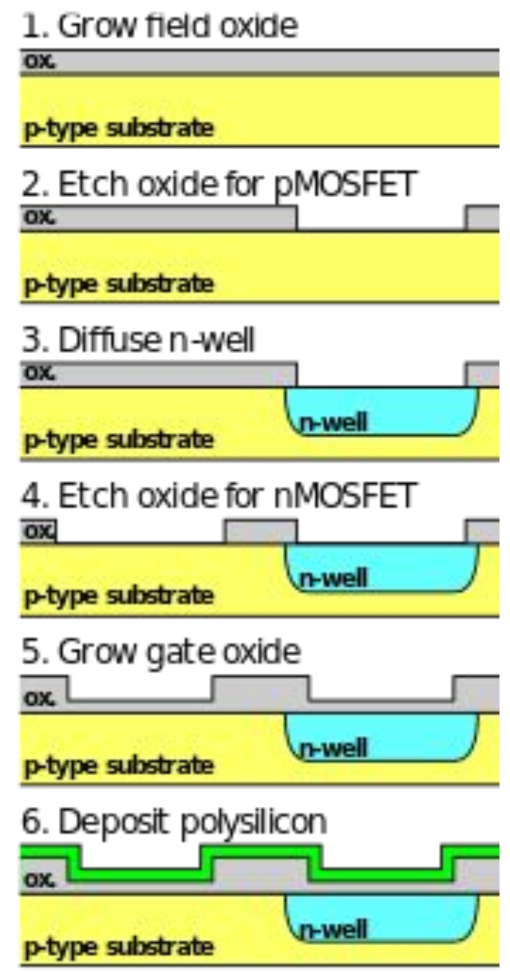
2. Dust

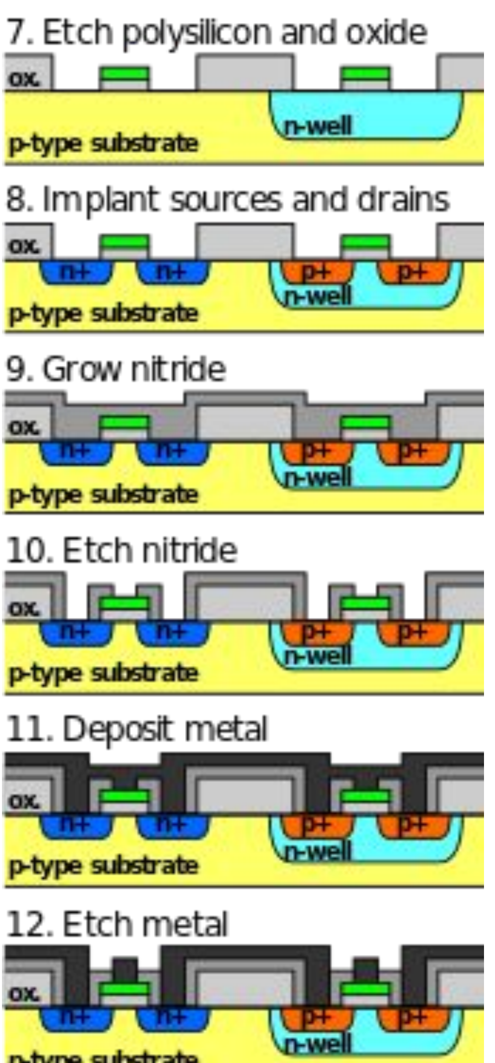
3. Process parameters (e.g., lateral diffusion)



4. Rough surfaces

Typical CMOS Process





Typical CMOS Process Layers

Layer	Key points:
Well (p,n)	N-well process p-type wafer (no p-well)
Diffusion	Diffusion (Active area) determines where transistors may go
Polysilicon	Poly overlapping with active = transistor
Select (p+,n+)	Select is where n+ and p+ ion implantation occurs; it can be used to place an opposite type region (e.g., put p+ select within n-well to create a p+ well plug, more later)
Contact To Poly Contact To Diffusion Via	All contacts/vias are the same size
LI, Metal1, Metal2	

Layers in the book's 0.25 um CMOS process

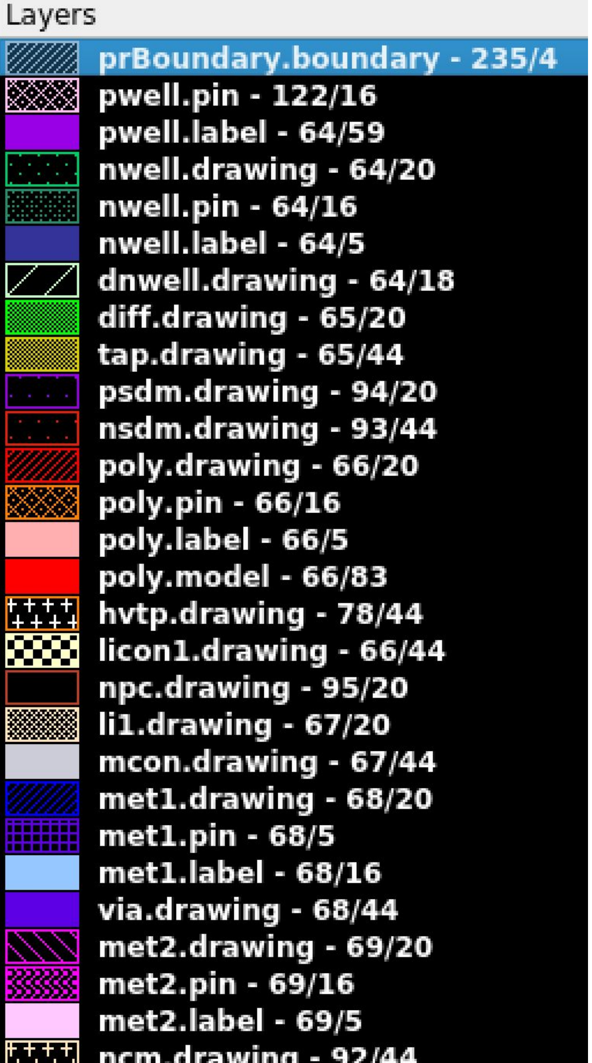
Layer Description	Representation				
metal	m1	m2	m3	m4	m5
well	nw				
polysilicon	poly				
contacts & vias	ct	v12,v23,v34,v45	nwc	pwc	
active area and FETs	ndif	pdif	nfet	pfet	
select	nplus	pplus	prb		

The book's process is NOT exactly the same as the one we will be using

Sky130 Layers

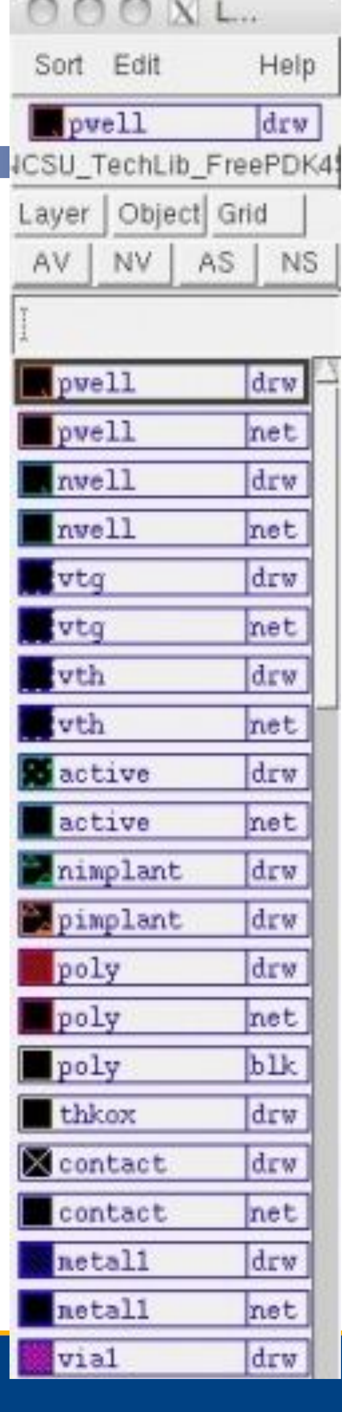
(Diagram not to scale!)

glass cut
11.8834
6.1346
0.54
5.2523
TOPOX K=3.9
0.09
PI1 K=2.94
0.4223
0.070
metal5
1.26
0.3777
TOPNIT K=7.5
0.505
via4
cap2m
via4
5.3711
NILD6 K=4.0
metal4
0.845
0.39
via3
capm
via3
4.0211
NILD5 K=4.1
metal3
0.845
0.42
via2
NILD4_C K=3.5
2.7861
NILD4 K=4.2
metal2
0.030
0.36
0.27
via1
NILD3_C K=3.5
2.0061
NILD3 K=4.5
metal1
0.030
0.36
0.265
0.075
NILD2 K=4.05
mcon
0.075
LINT K=7.3
1.3761
LINT K=7.3
li
0.1
0.4299
licon
IOX K=3.9
1.0111
PSG K=3.9
field poly
0.6099
licon
SPNIT K=7.5
0.121
0.9361
polysilicon gate
0.18
0.3262
FOX K=3.9
0.0
diffusion
0.12
nwell
p-substrate
0.0431
0.006



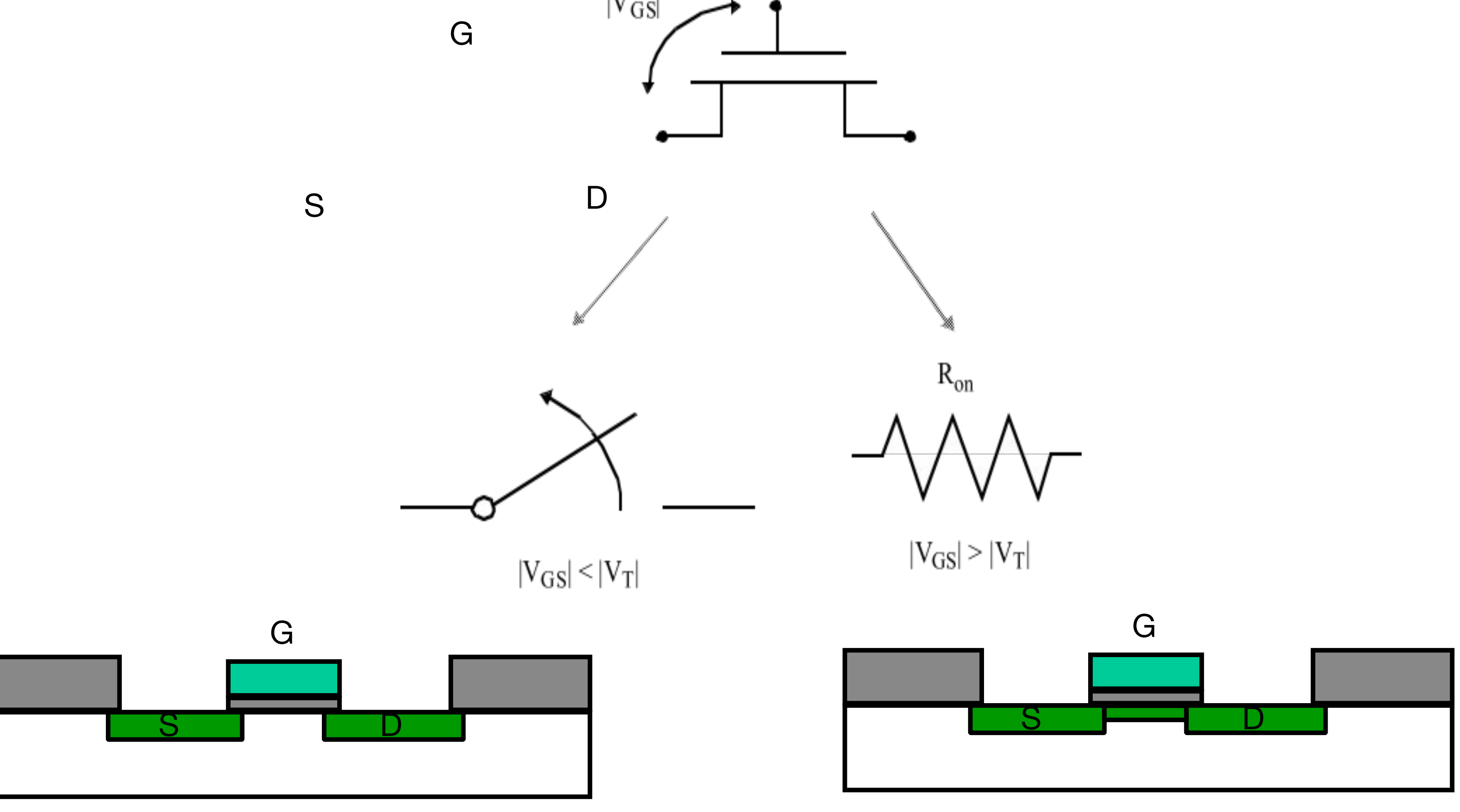
A 45nm Process

- NOTE: drw vs net – use drawing
- pwell/nwell – wells to make tx
- vtg/vth – extra implant for high Vth
- active – define tx (no field oxide)
- n/p implant – makes source/drain
- poly – tx gate and routing
- thkox – thick oxide for high Vdd tx
- contact – hole from metal1 to poly/diff
- metaln/vian – metal and via layer n



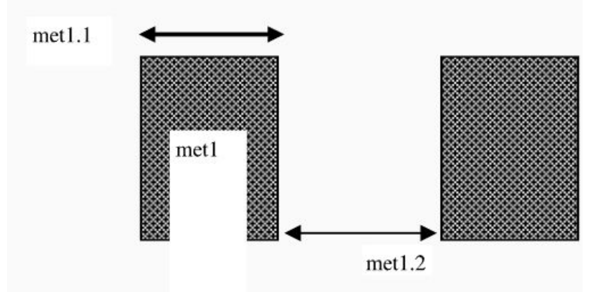
Cadence Virtuoso

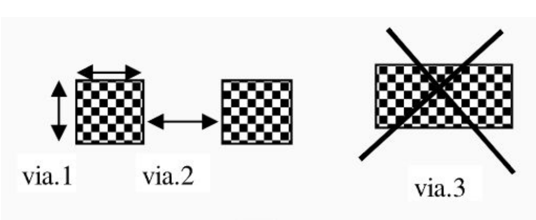
Basic Field-Effect Transistor



Intra-Layer Design Rules

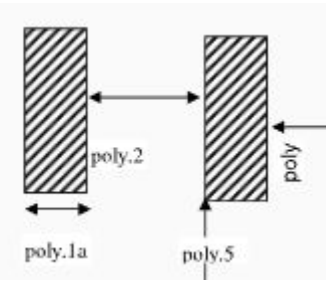
- Minimum dimensions (e.g., widths) of objects on each layer to maintain that object after fab
  - minimum line width is set by the resolution of the patterning process (photolithography)
- Minimum spaces between objects (that are *not* related) on the same layer to ensure they will not short after fab
- Exact dimensions

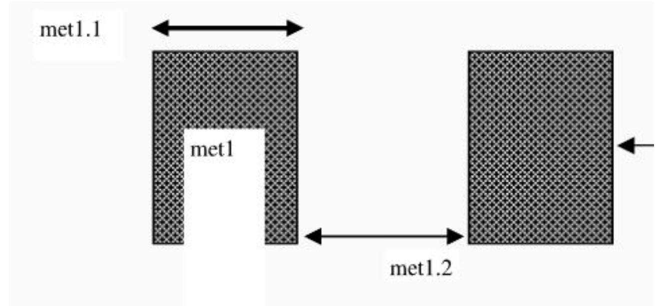


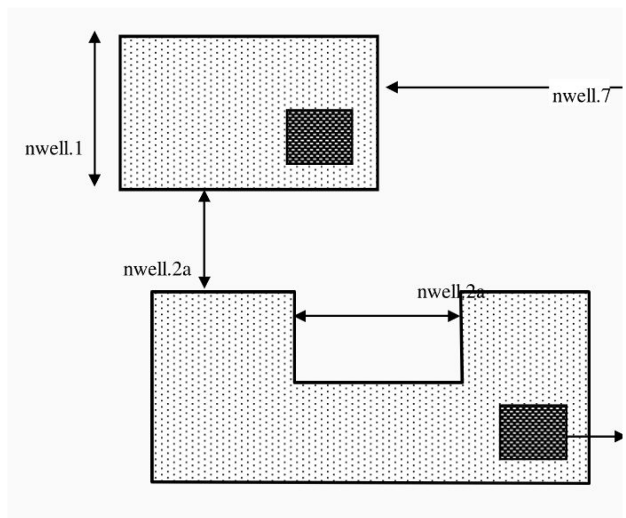


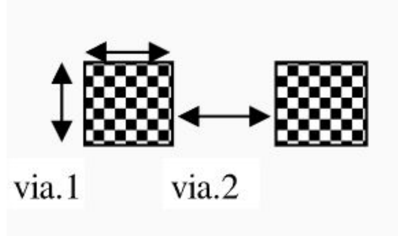
(m1.1)	Width of metal1	0.140	µm
(m1.2)	Spacing of metal1 to metal1	0.140	µm

(Some) Intra-Layer Rules



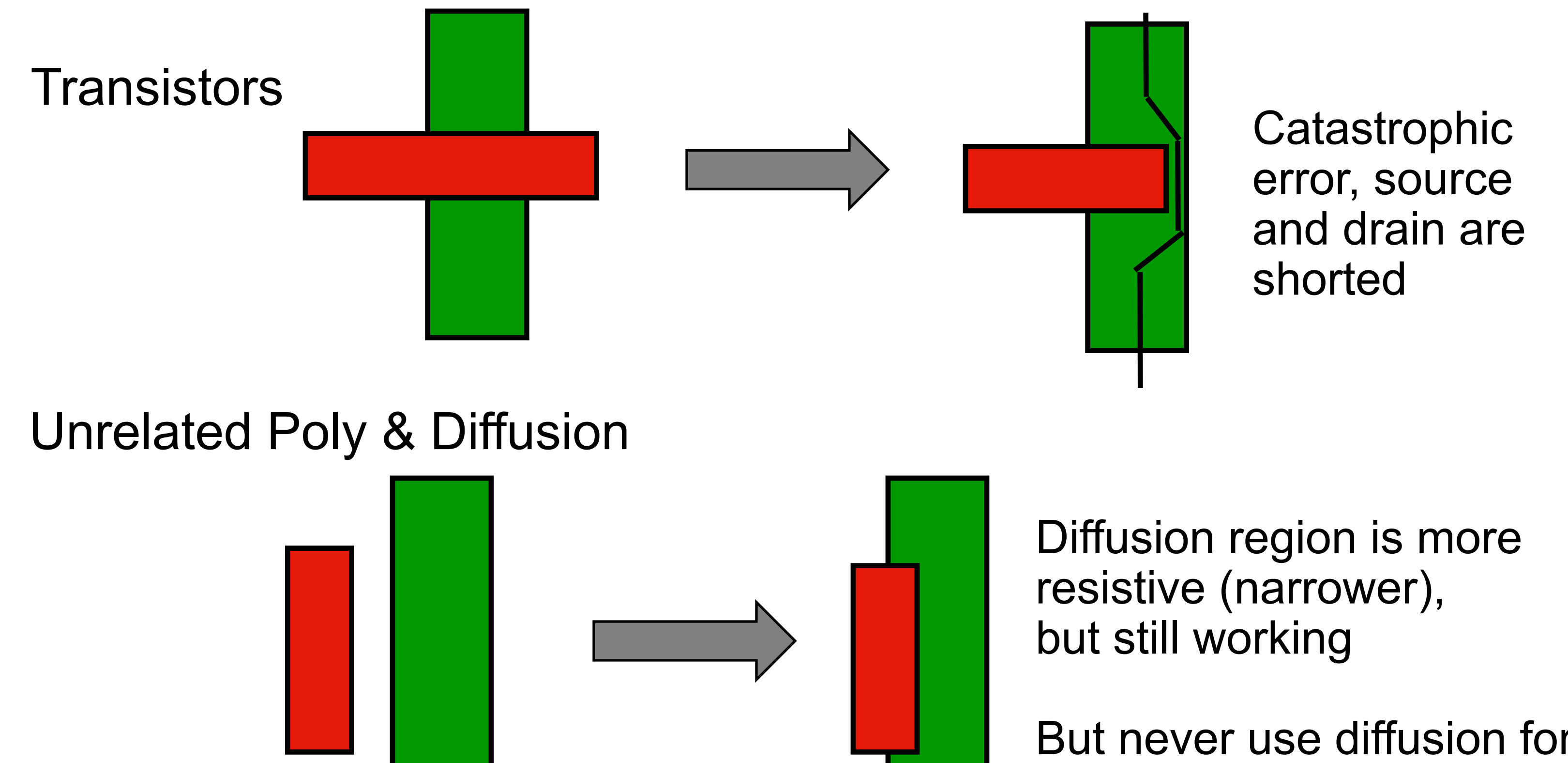




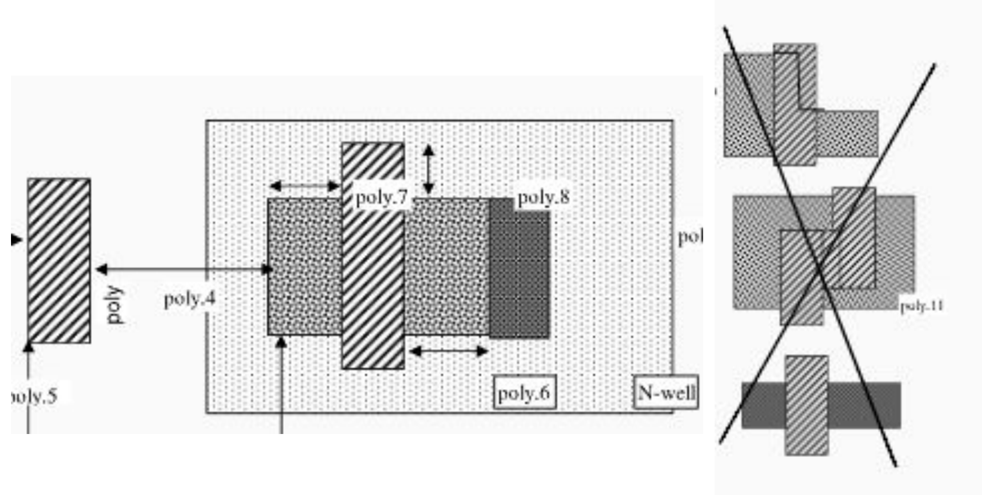


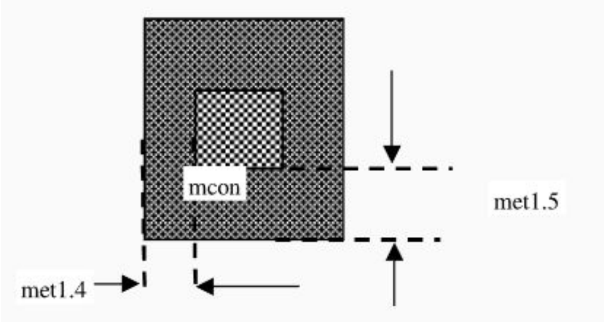
Inter-Layer Design Rules

Transistor rules – transistor formed by overlap of diffusion (also called active) and poly layers



(Some) Inter-Layer Rules

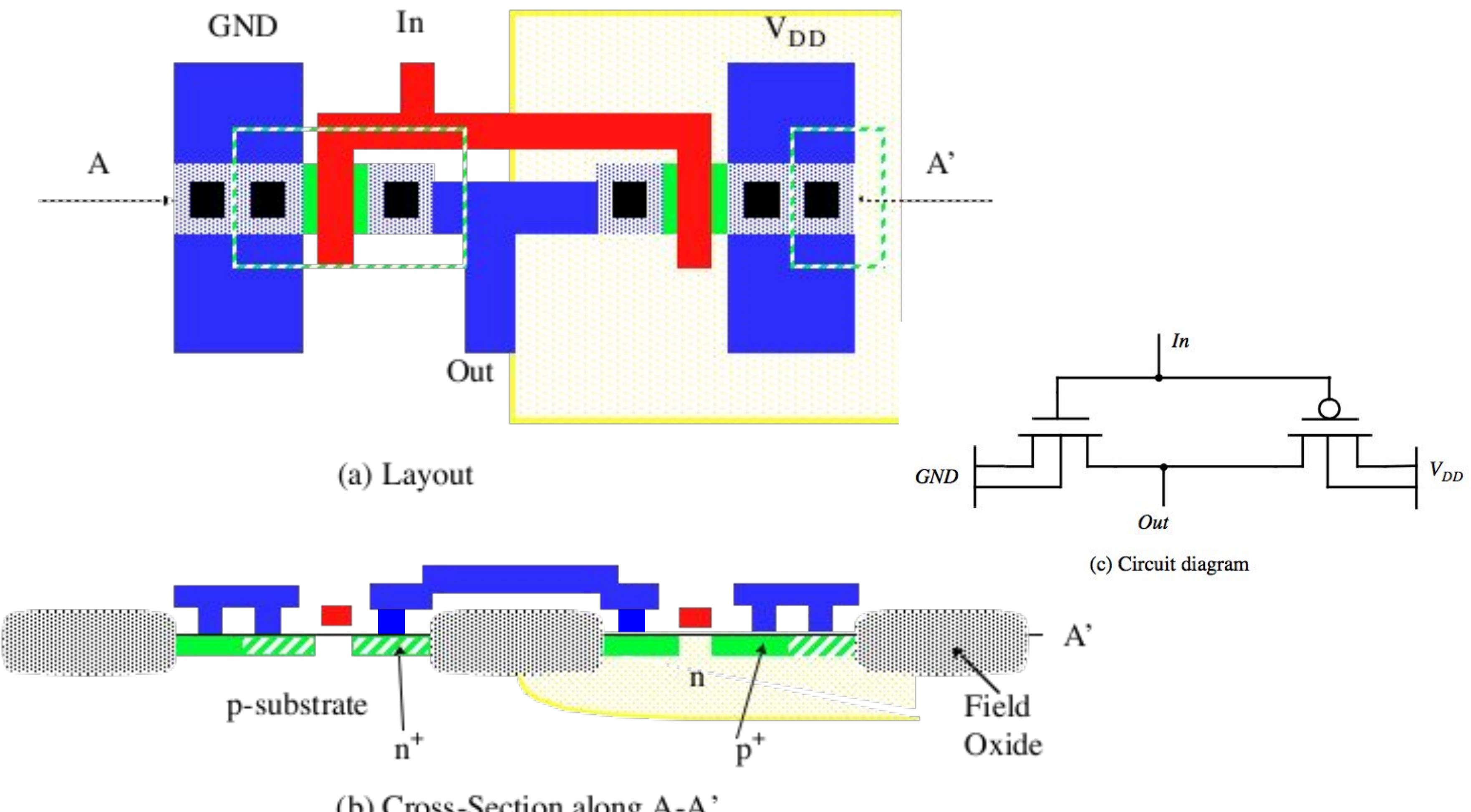




Rule	Description	Flags	Value	Unit
(poly.4)	Spacing of poly on field to diff (parallel edges only)	P	0.075	µm
(poly.5)	Spacing of poly on field to tap	P	0.055	µm
(poly.6)	Spacing of poly on diff to abutting tap (min source)	P	0.300	µm
(poly.7)	Extension of diff beyond poly (min drain)	P	0.250	

Rule	Description	Flags	Value	Unit
(m1.4)	Mcon must be enclosed by Met1 by at least ... (Rule exempted for cell names documented in rule m1.4a)	P	0.030	µm
(m1.4a)	Mcon must be enclosed by Met1 by at least (for cell names “s8cell_ee_plus_sseln_a”, “s8cell_ee_plus_sseln_b”, “s8cell_ee_plus_sselp_a”, “s8cell_ee_plus_sselp_b”, “s8fpls_pl8”, and “s8fs_cmux4_fm”)	P	0.005	µm
(m1.5)	Mcon must be enclosed by Met1 on one of two adjacent sides by at least ...	P AL	0.060	µm

CMOS Inverter Layout

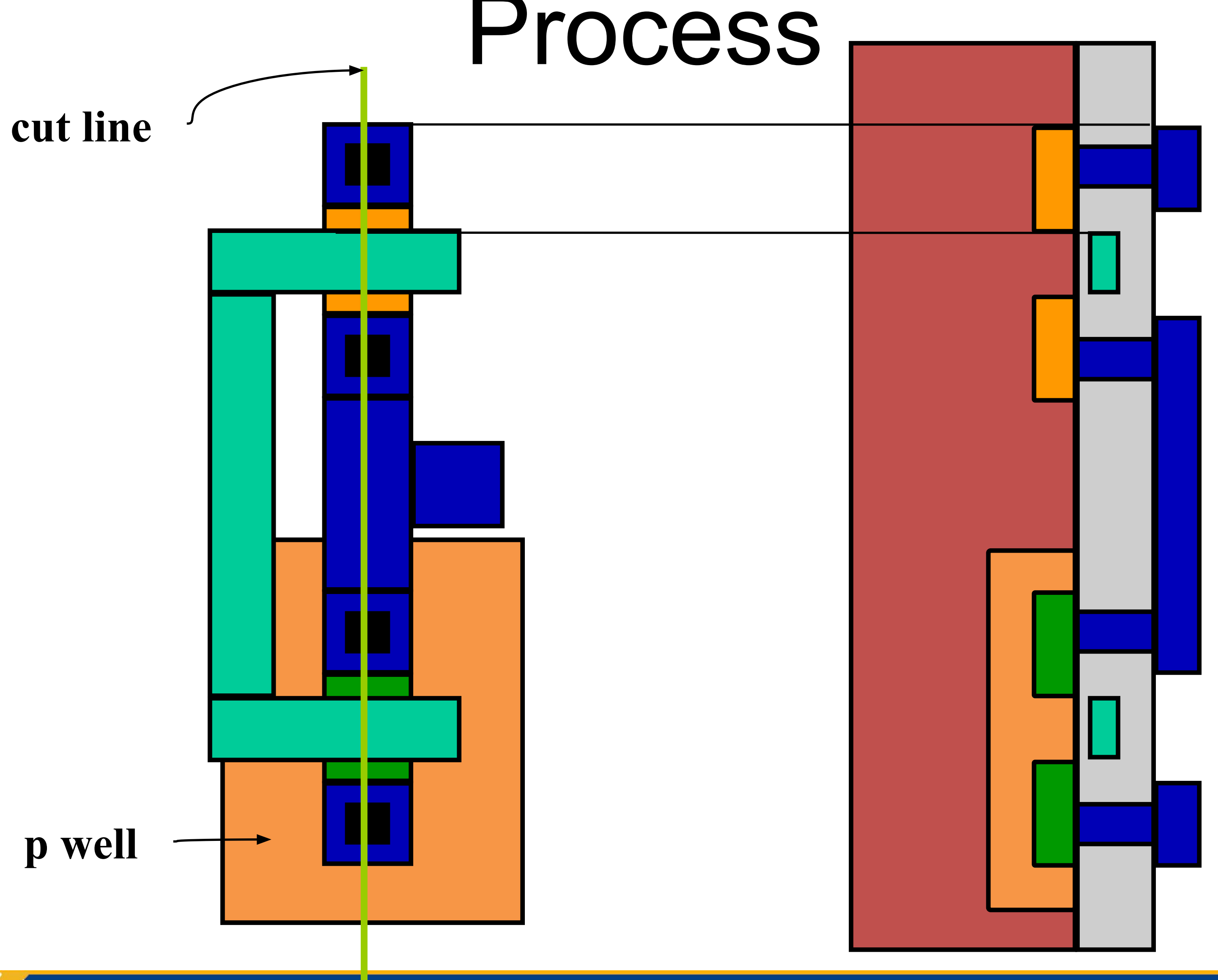


(a) Layout

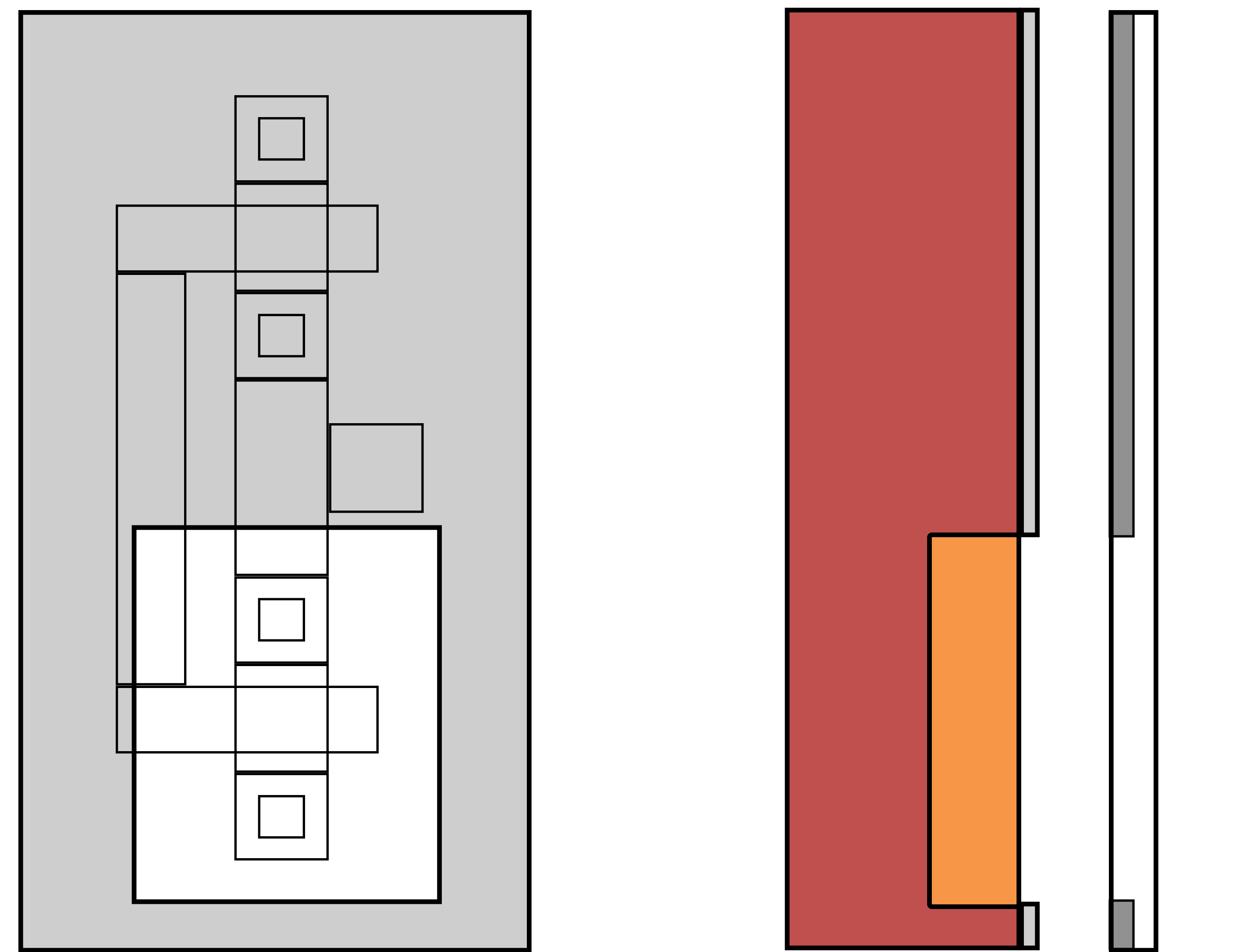
(c) Circuit diagram

(b) Cross-Section along A-A'

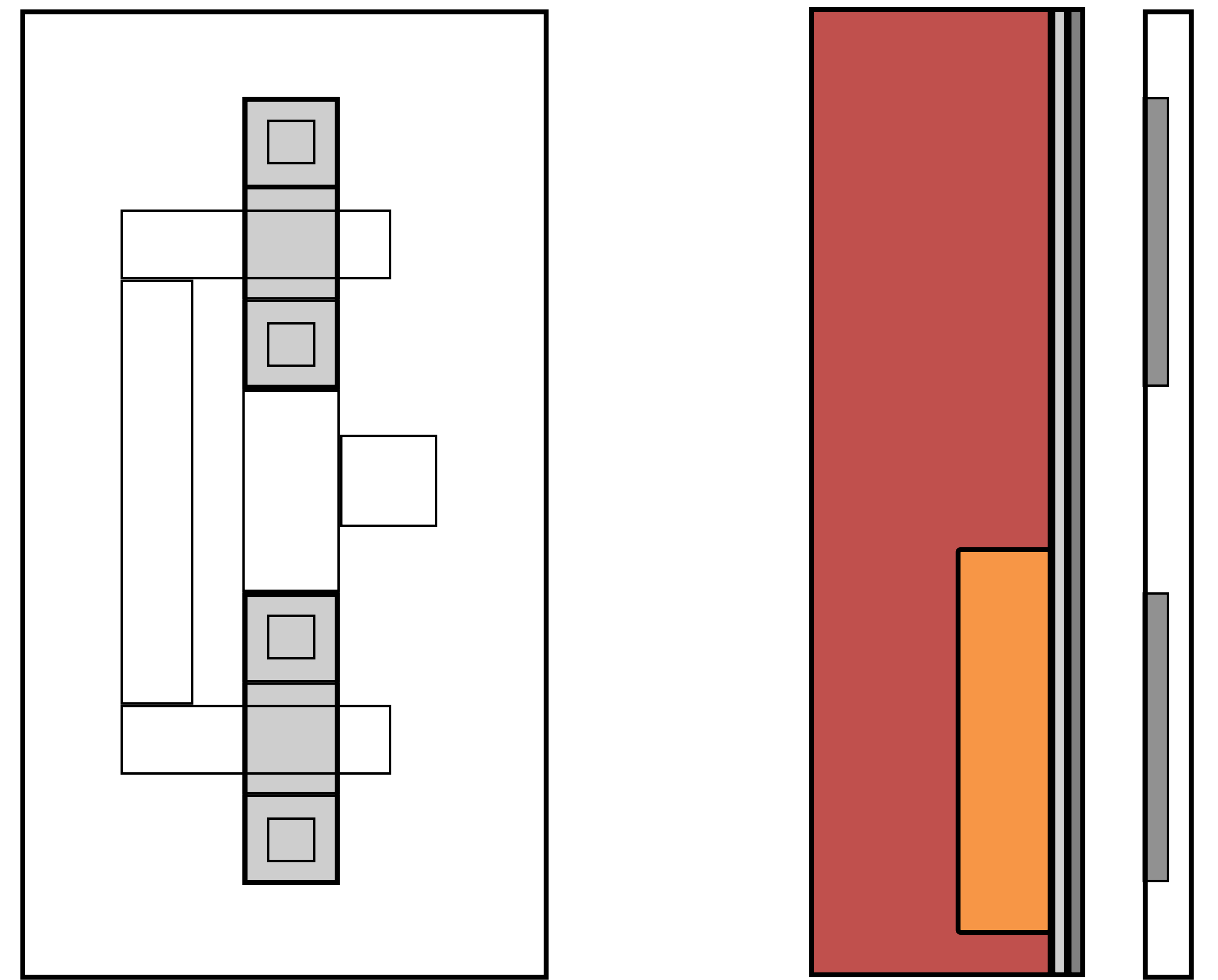
Simplified CMOS Inverter Process



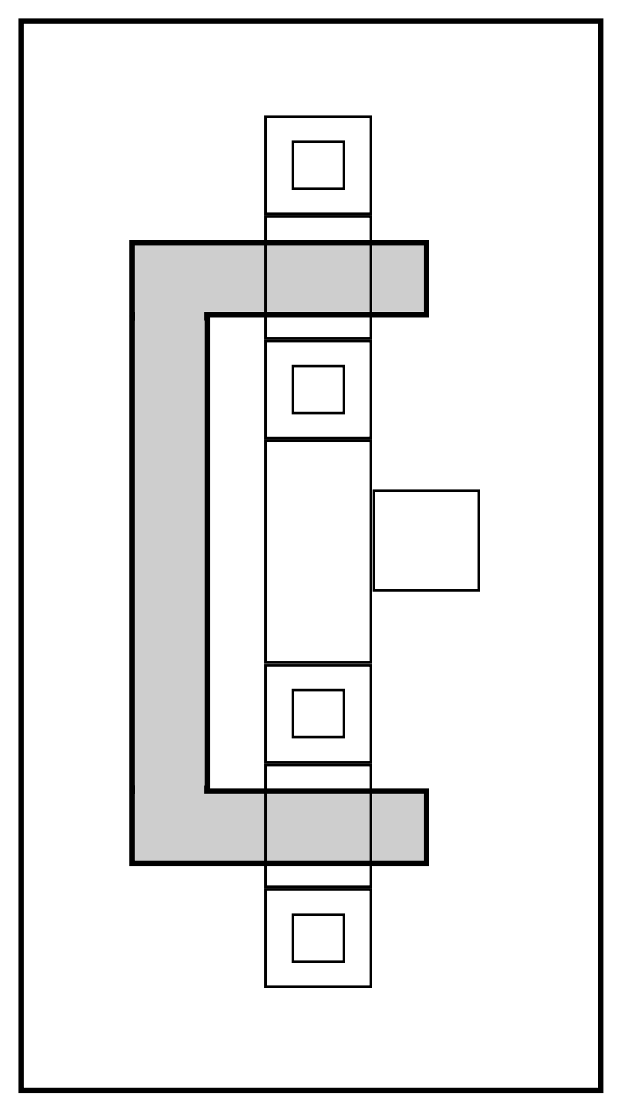
P-Well Mask (pwell or nwell)

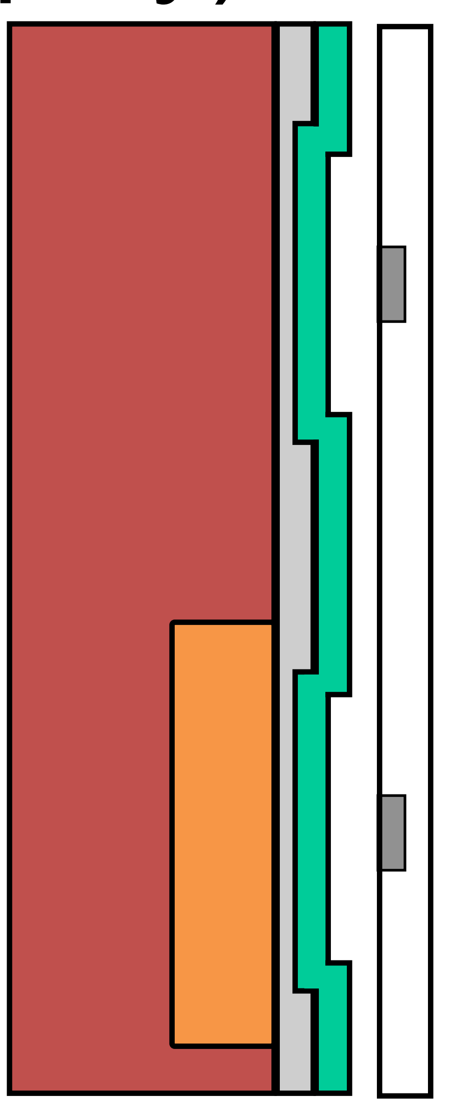


Active Mask (diff)

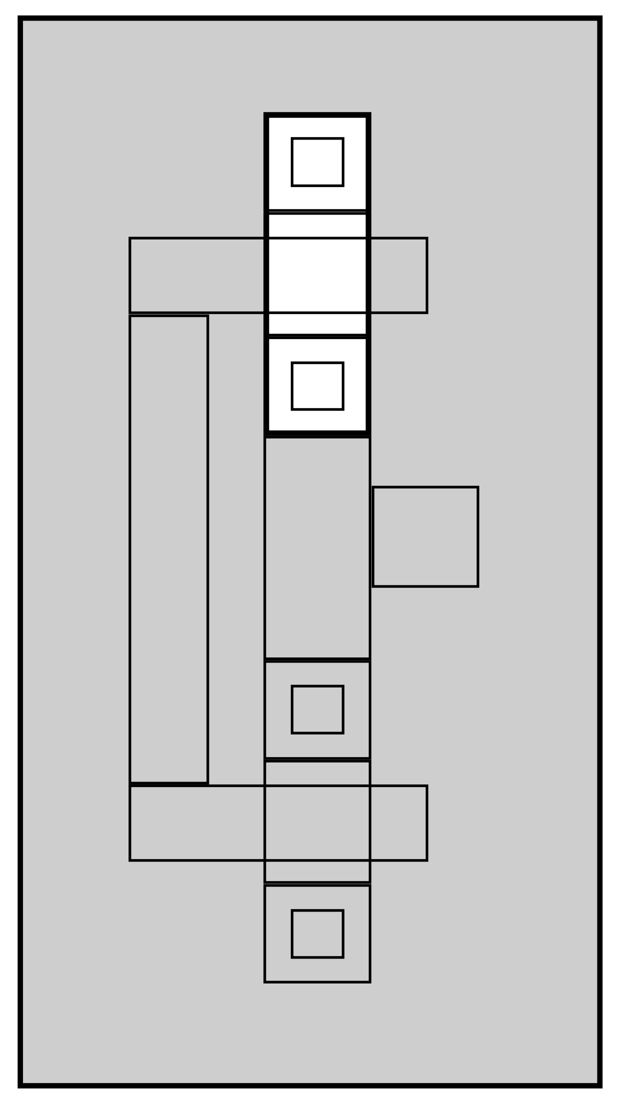


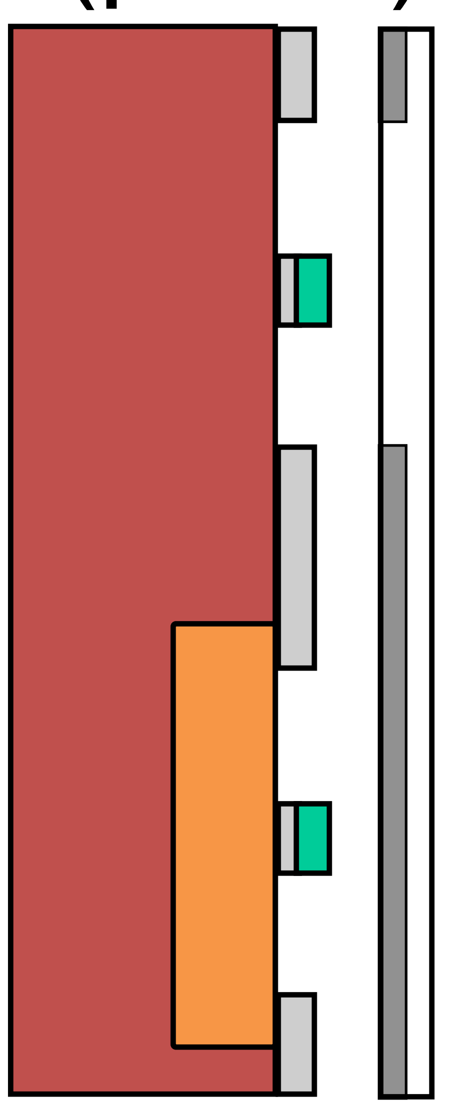
Poly Mask (poly)



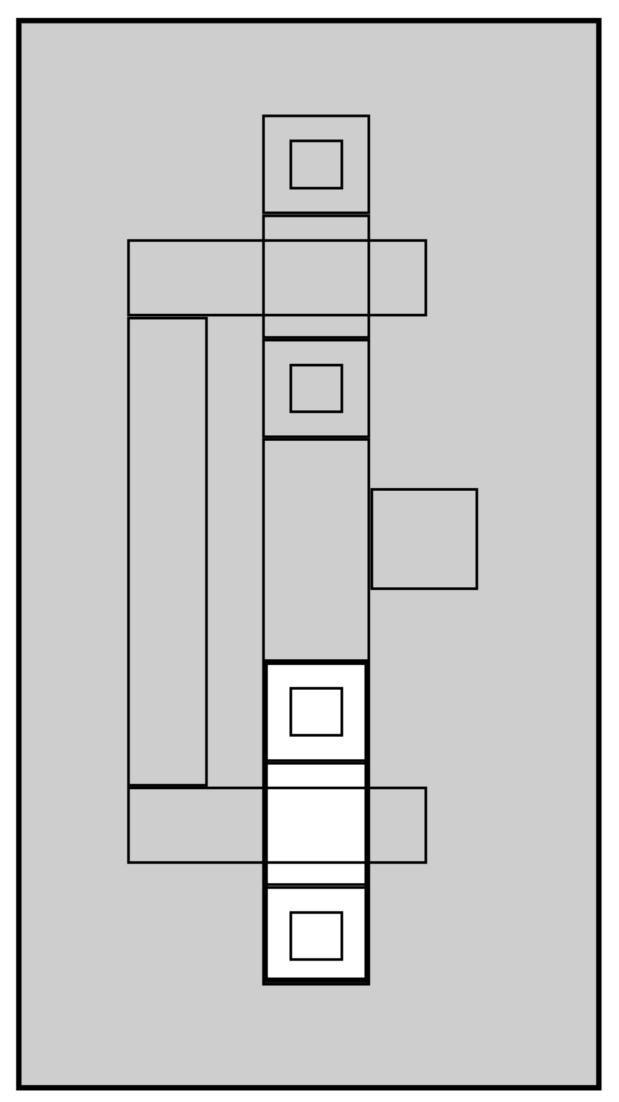


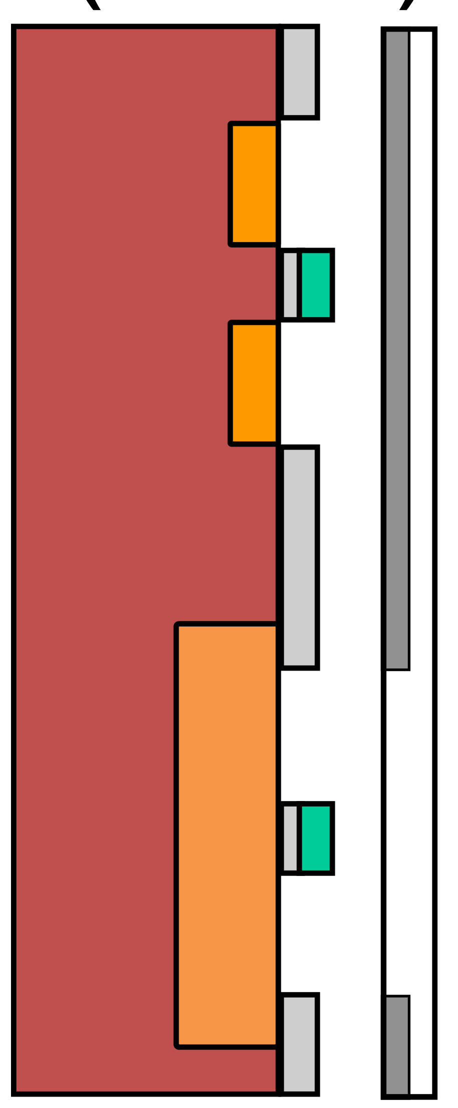
P+ Select Mask (psdm)



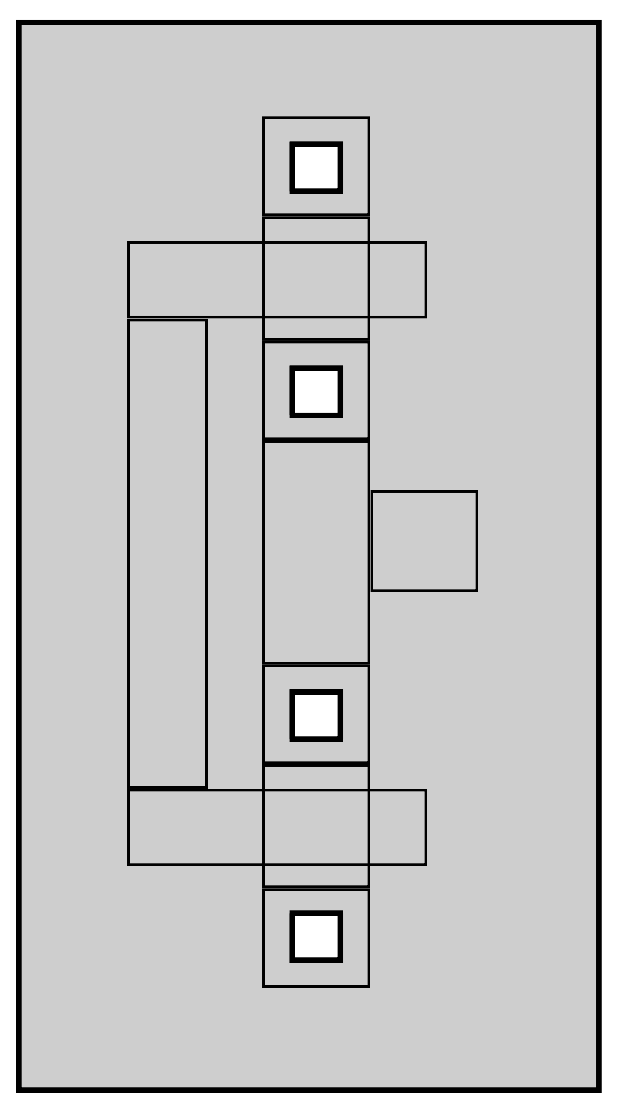


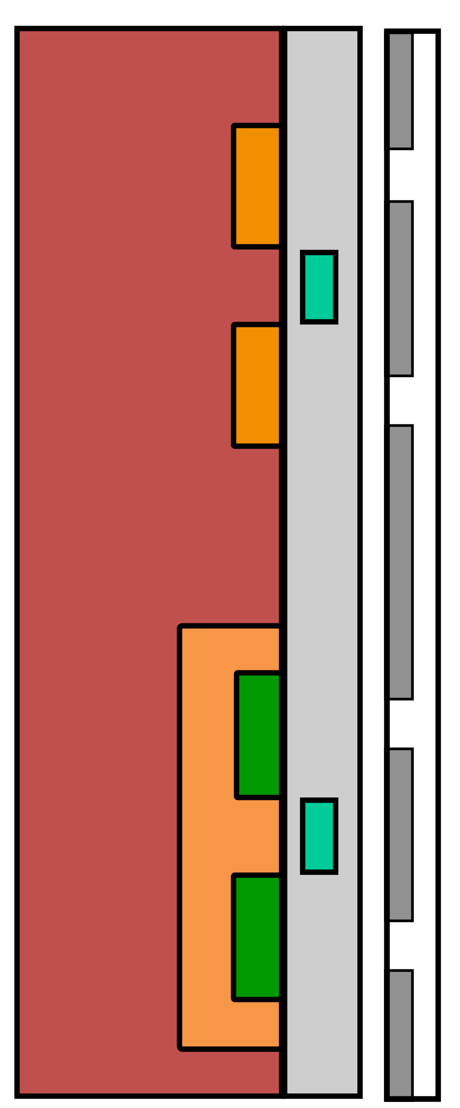
N+ Select Mask (nsdm)



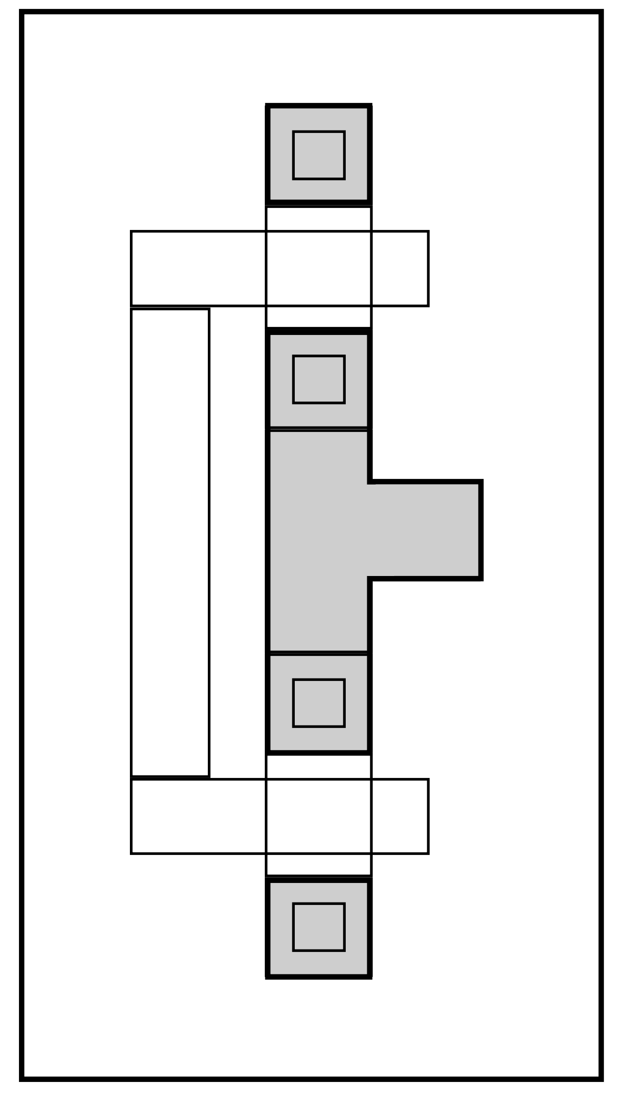


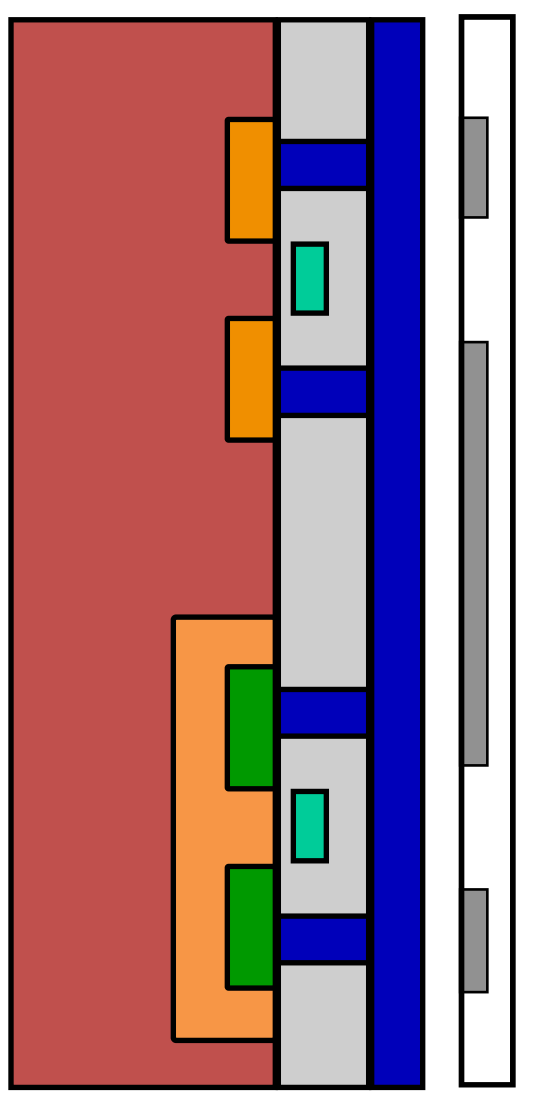
Contact Mask (licon+npc)





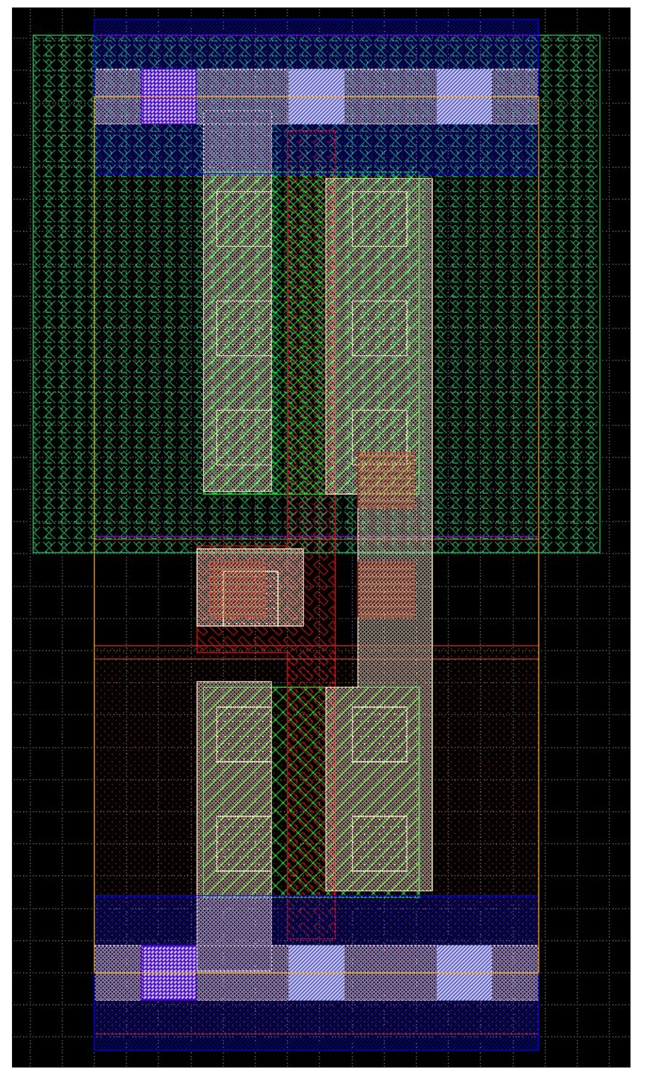
Metal Mask(m1)



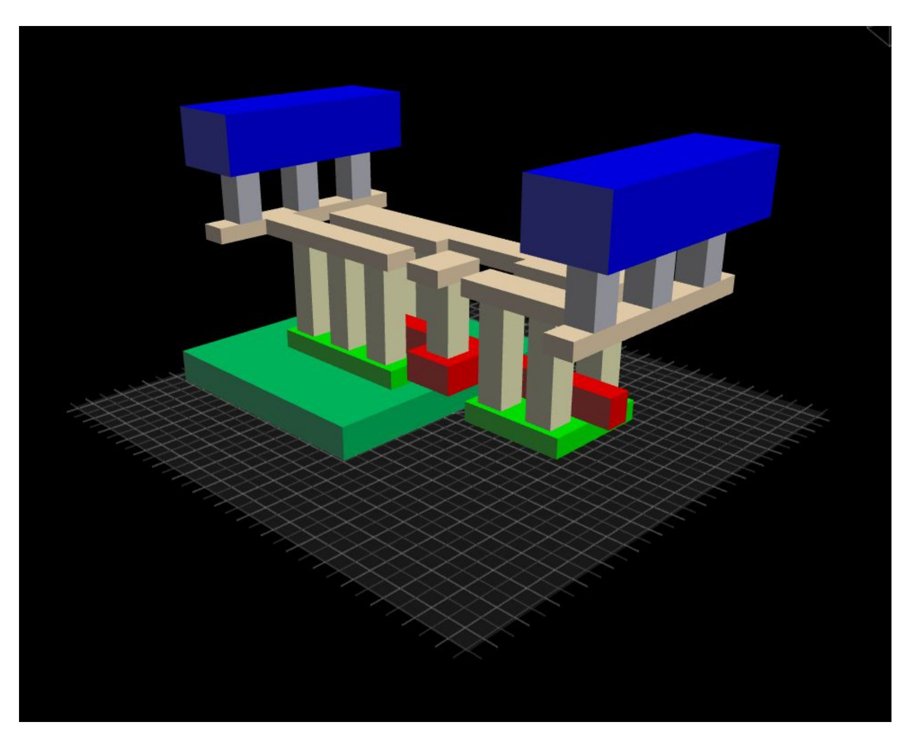


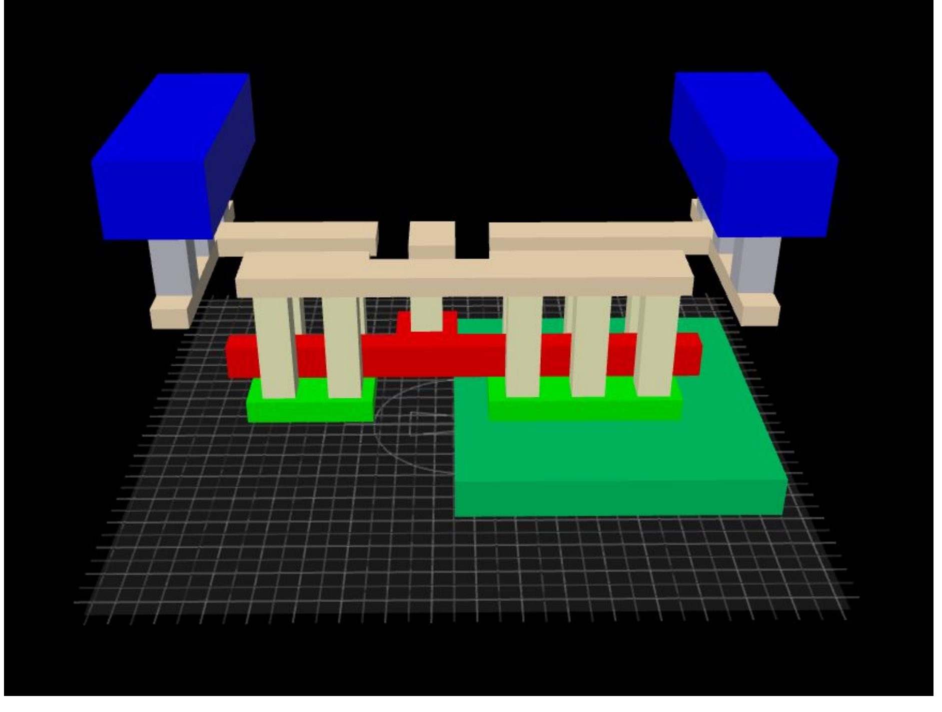
Example Layout: INV1

- Horizontal n-diffusion and p-diffusion strips
- Vertical polysilicon gates
- Metal1 V_{DD} rail at top
- Metal1 GND rail at bottom

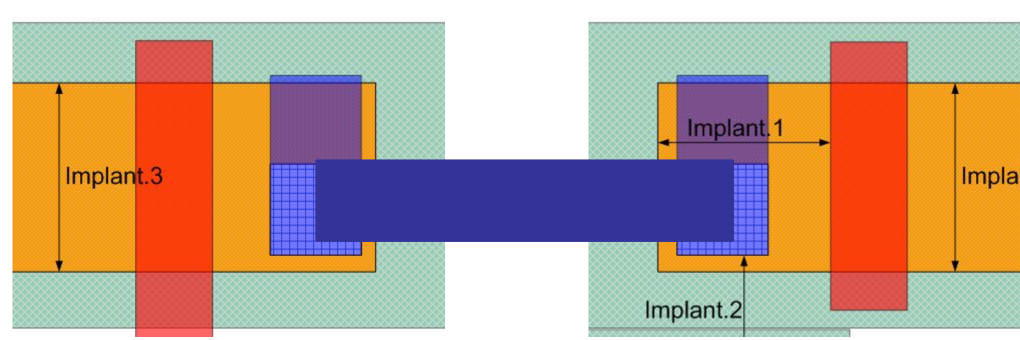


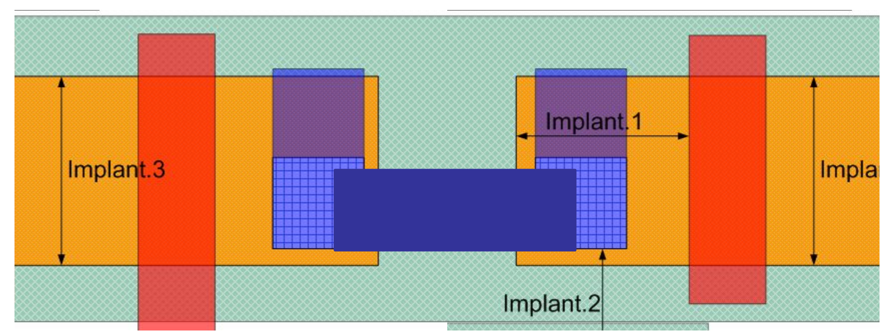
2.5D Views

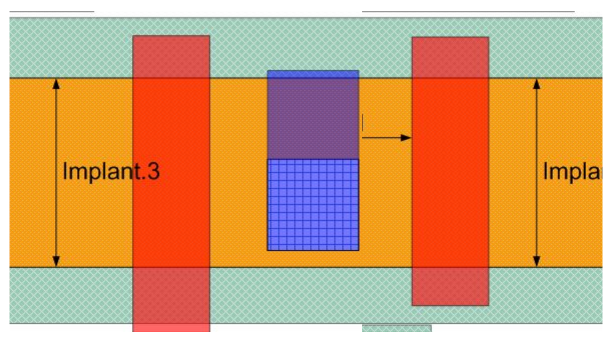


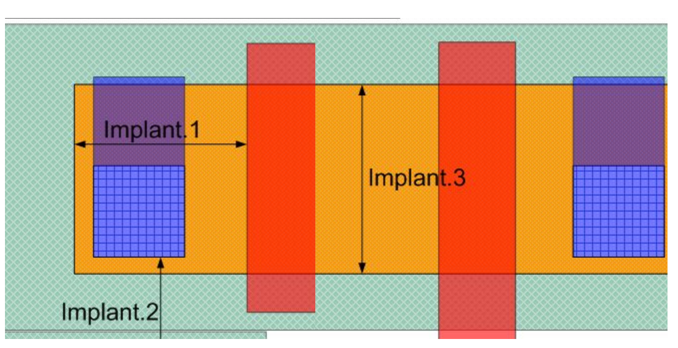


Well and Diffusion Sharing

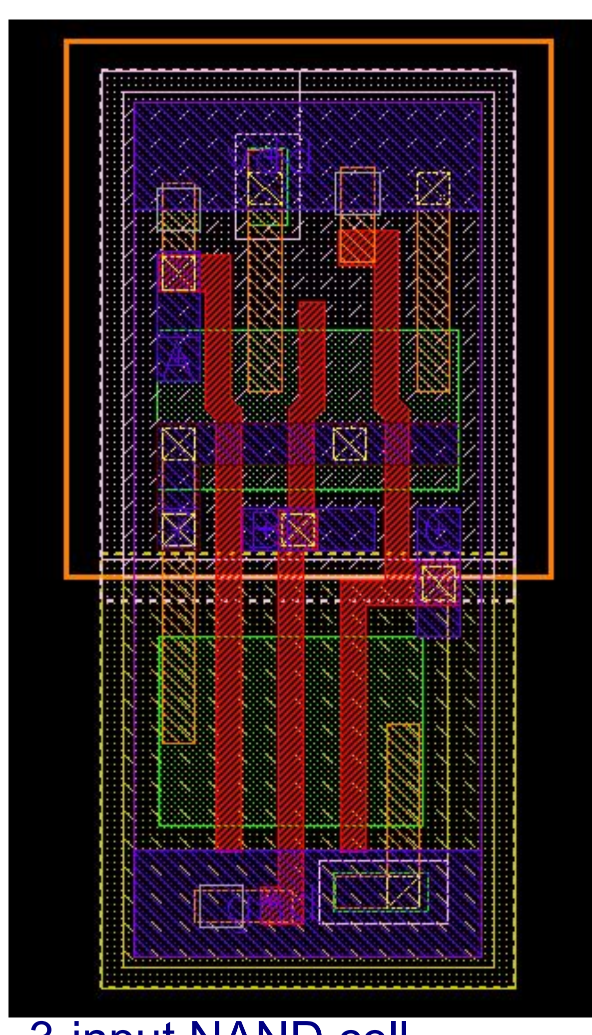




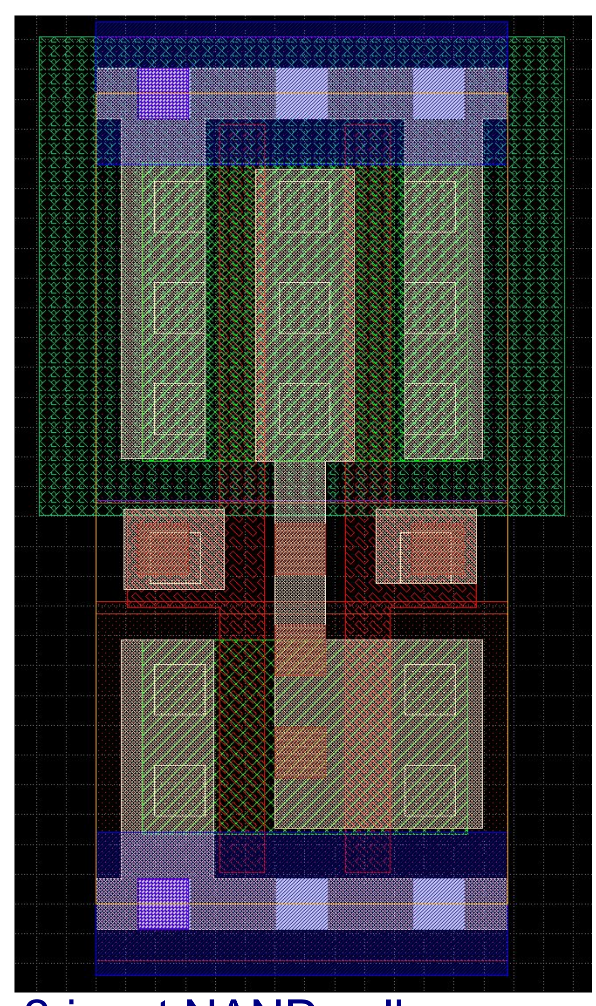




Standard Cell - Example



3-input NAND cell
(from ST Microelectronics):



2-input NAND cell
(from Skywater 130nm):

Next Lecture

- Devices and CMOS