

# Lecture 02: Fabrication

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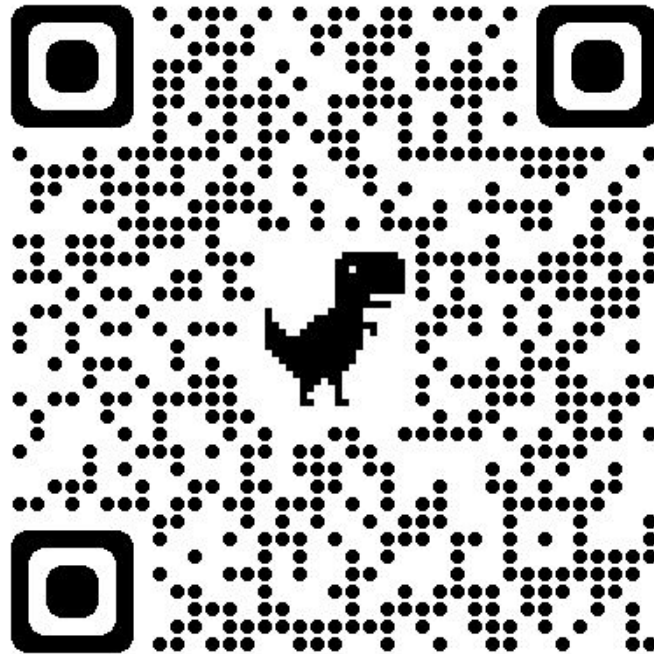
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UCSC, Computer Science & Engineering  
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mrg@ucsc.edu



# Syllabus

- <https://vlsida.github.io/cse122-222a-s23/syllabus.html>

• **This is a project class!**



# Today's Lecture

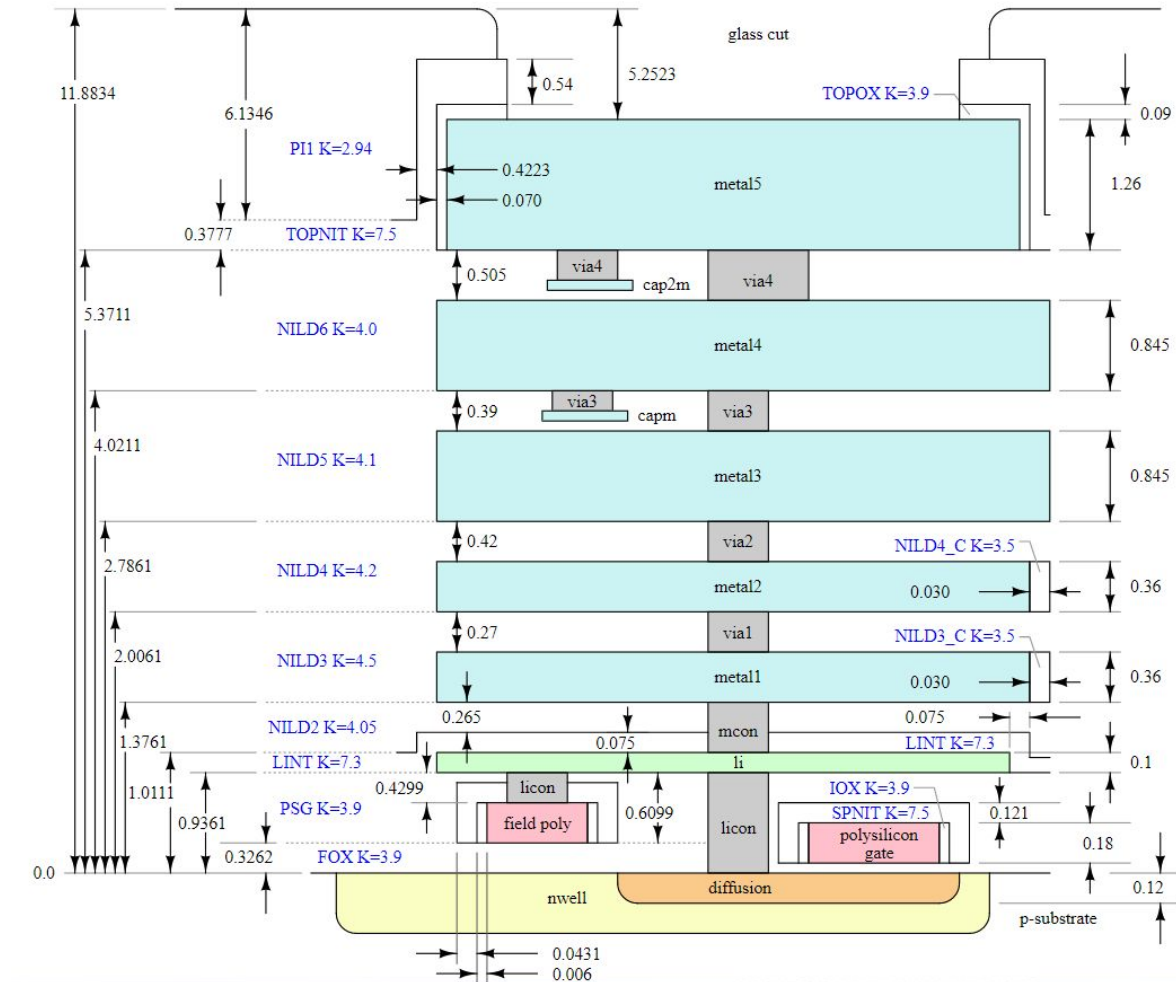
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- Semiconductor Material types
- Packaging and Dies
- Basic steps of semiconductor processing
  - Photolithography
  - Oxidation/Etching/Implantation/Deposition
  - Planarization
- 

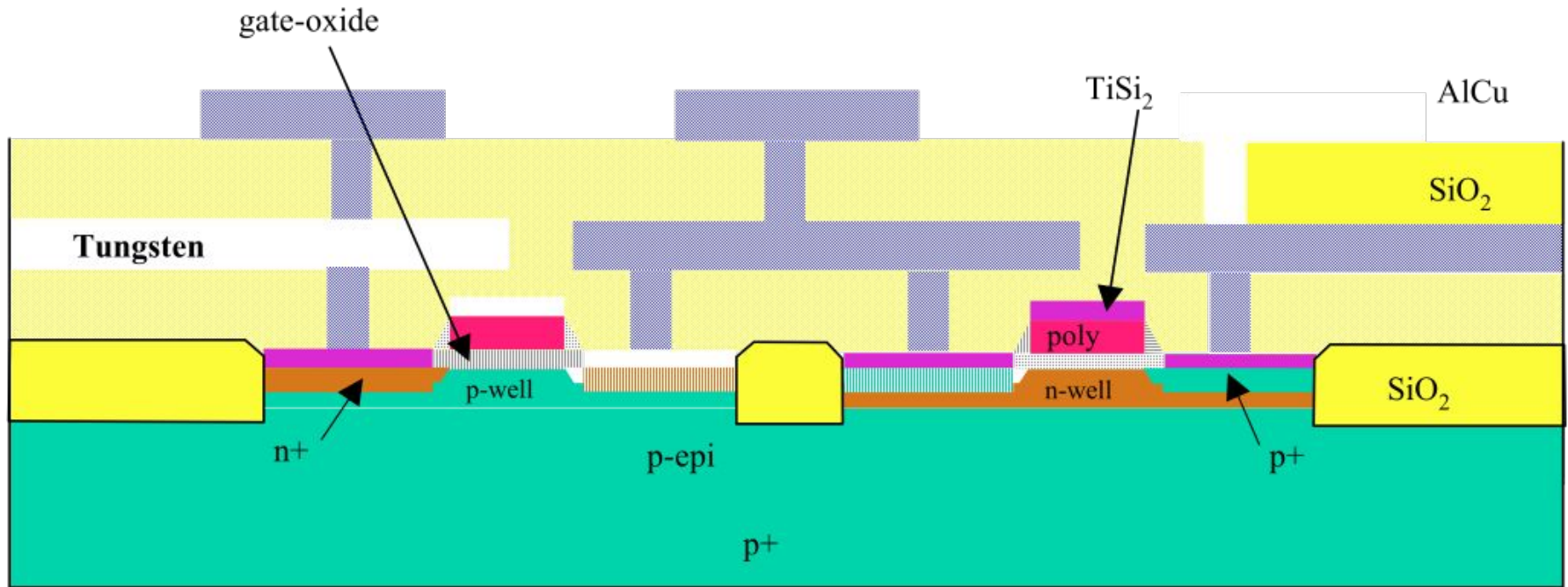


# Skywater 130nm

(Diagram not to scale!)



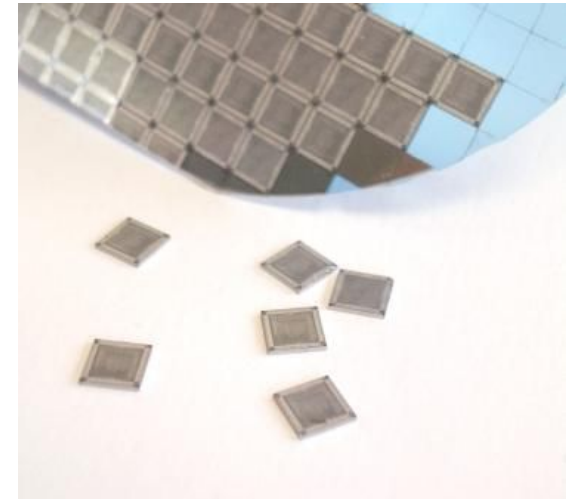
# A “Modern” CMOS Process



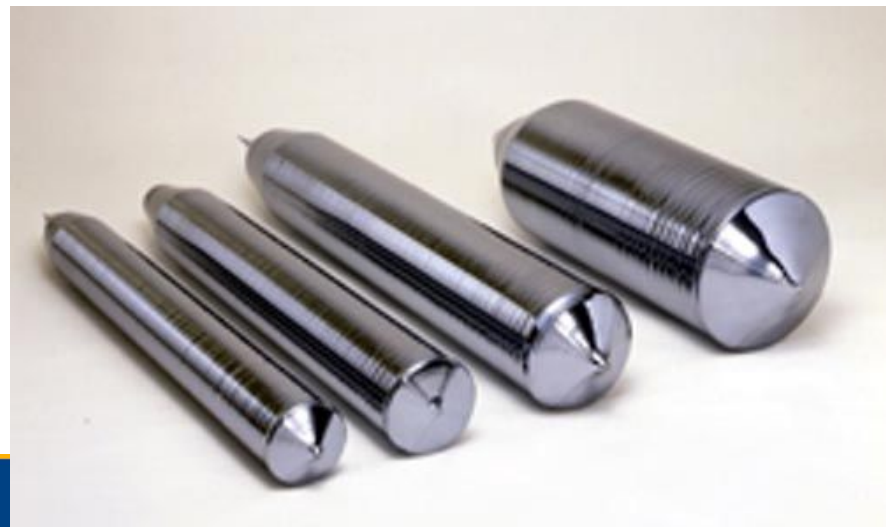
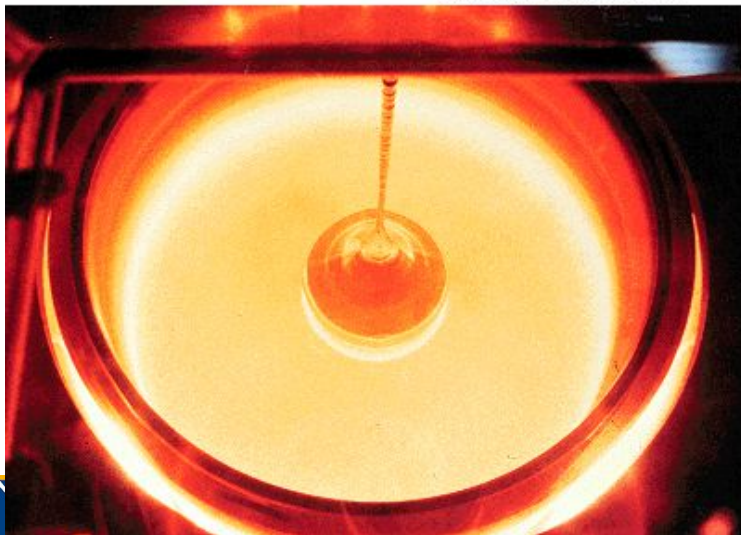
Dual-Well Trench-Isolated CMOS Process

# The Wafer

- 450mm wafer size (18 in)
- P-type Silicon

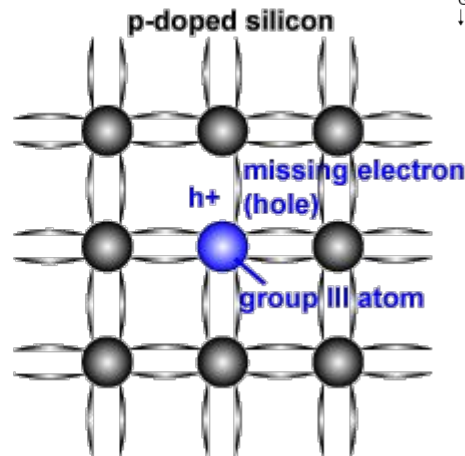
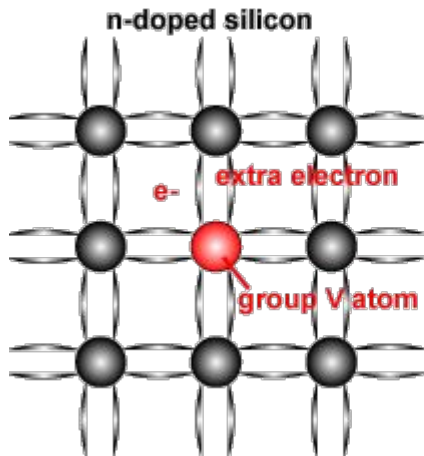


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# N and P-type Silicon

- Silicon has 4 electrons in outer shell
- N-type has “extra” electrons
  - E.g. Phosphorous, group V atom
- P-type has “extra” holes
  - E.g. Boron, group III atom



Group →	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
↓ Period																		
1	1 H																	2 He
2	3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
3	11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
4	19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
5	37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
6	55 Cs	56 Ba		72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
7	87 Fr	88 Ra		104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 Ds	111 Rg	112 Cn	113 Uut	114 Fl	115 Uup	116 Lv	117 Uus	118 Uuo
Lanthanides	57 La	58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu			
Actinides	89 Ac	90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr			



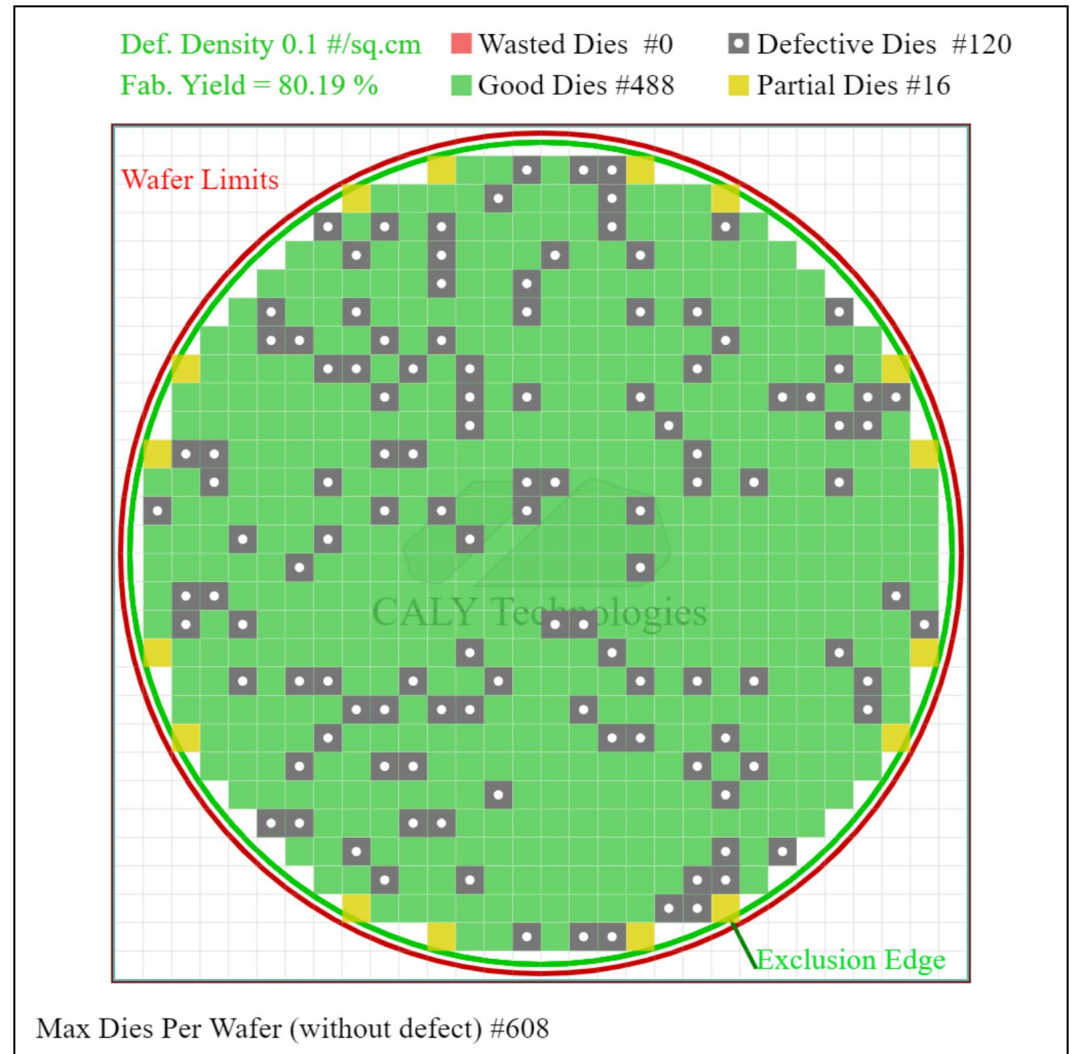
# Wafer Yield

15mm x 15mm

18in wafer

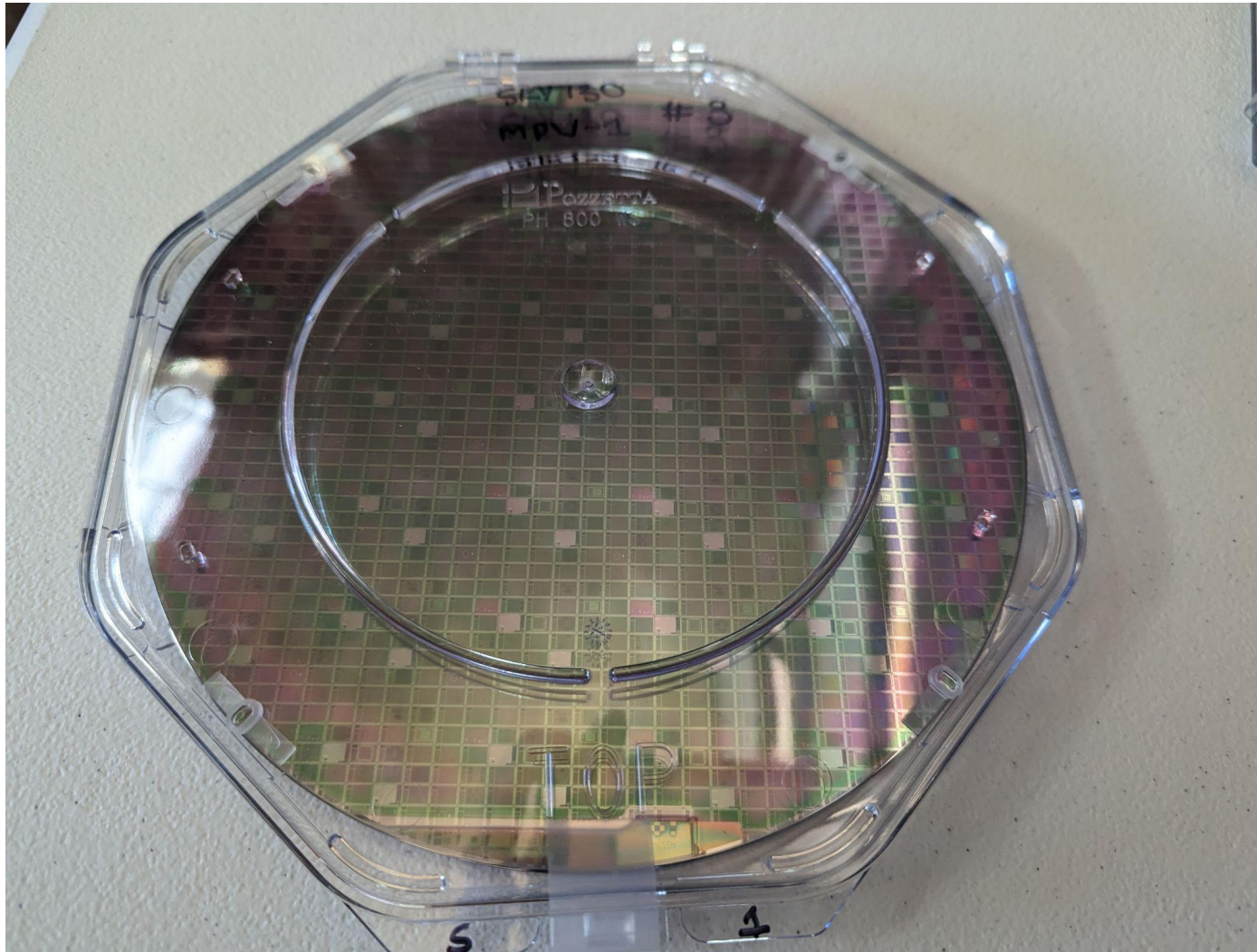
Loss

- Scribe lines
- Edges
- Defects



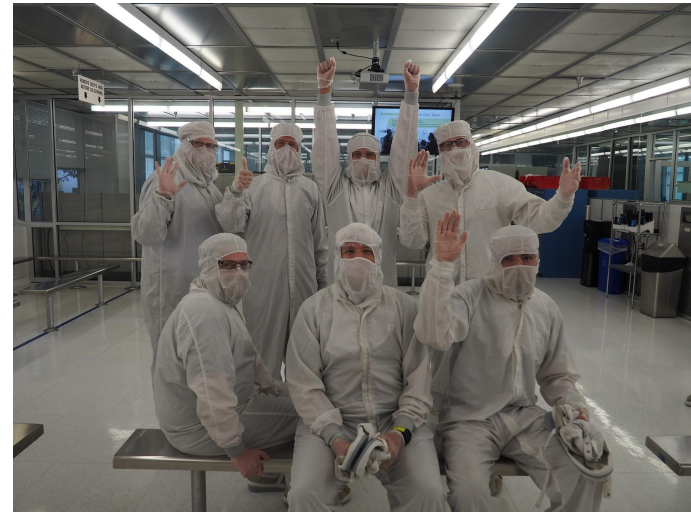


# Skywater 130nm Wafer

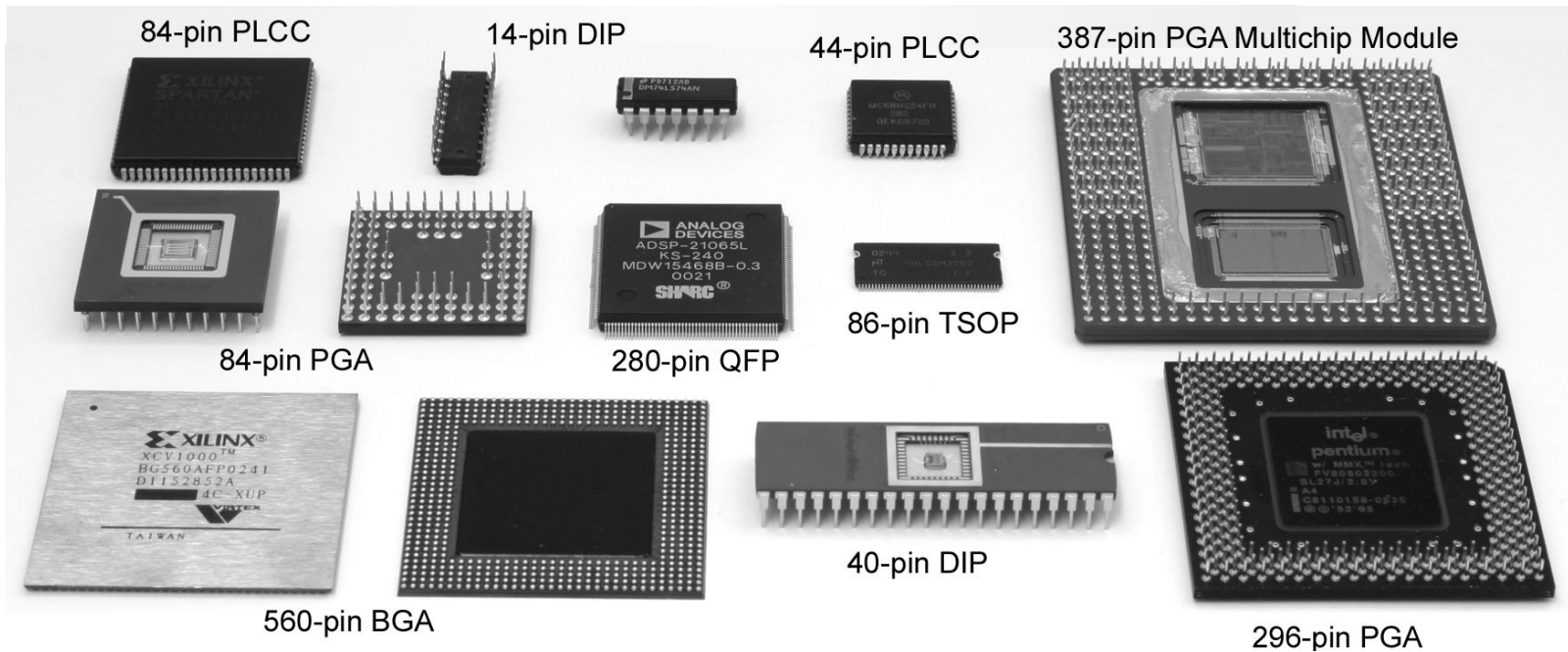


# Clean Rooms

- Class 100, 1000, ...
  - 0.5um per ft<sup>3</sup>
- Often “hoods” for very clean areas
- Particles cause defects...
- Bunny suits

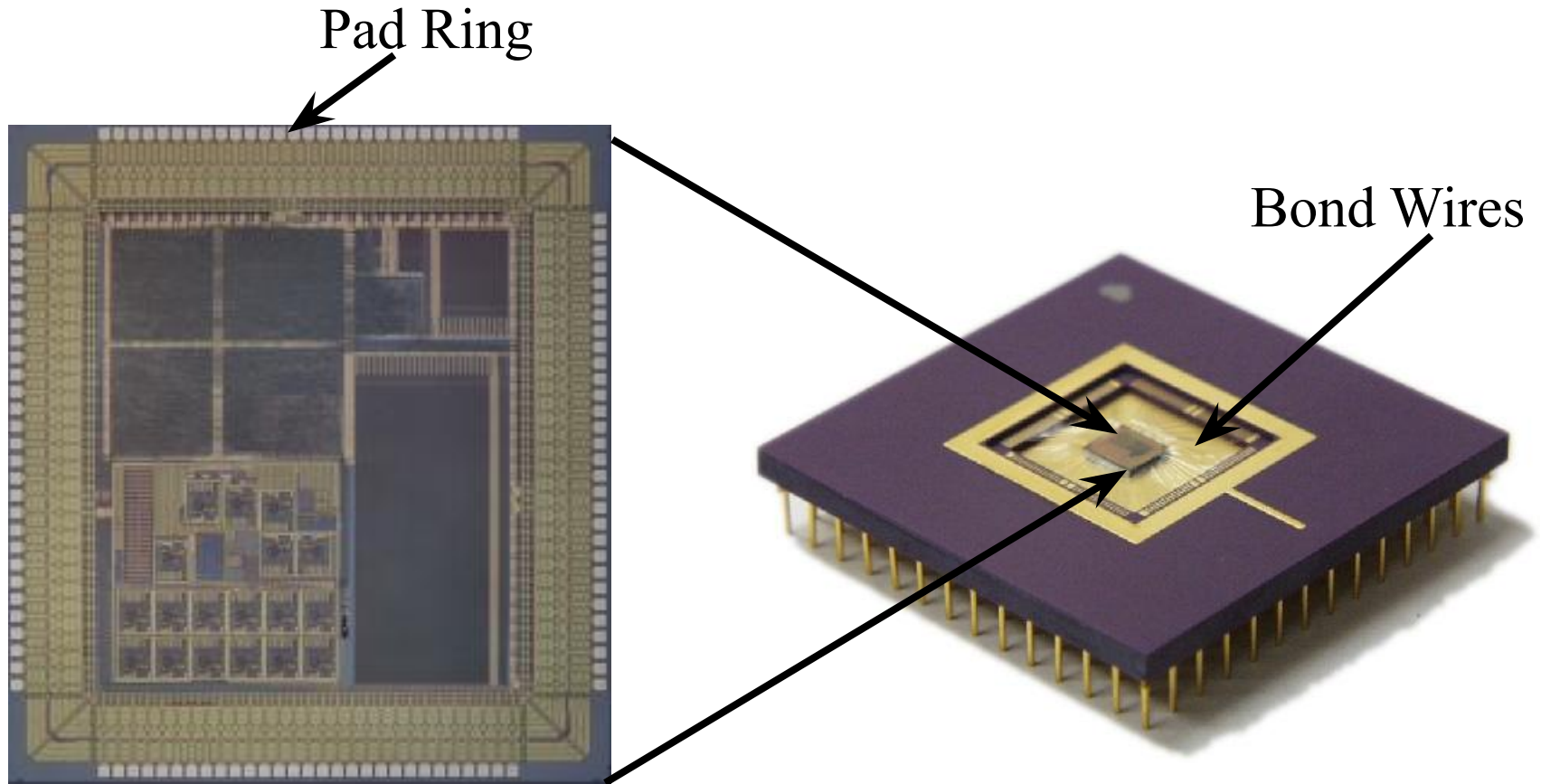


# Package Types





# Pin Grid Array (PGA) Package

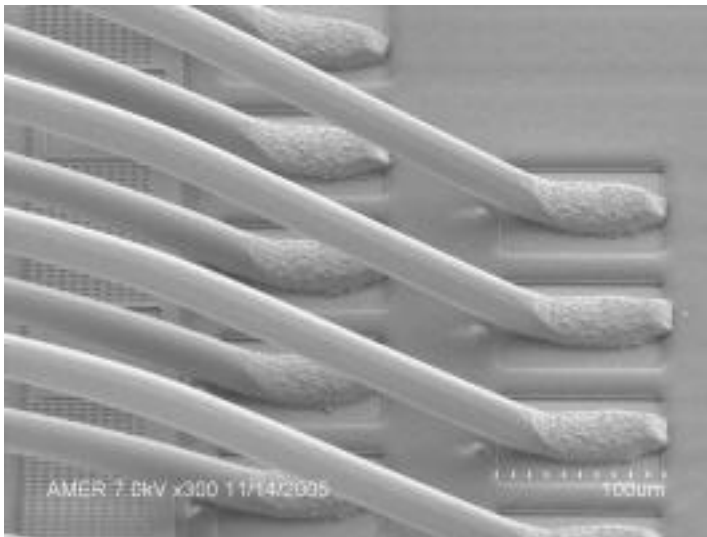


# Bond Wires

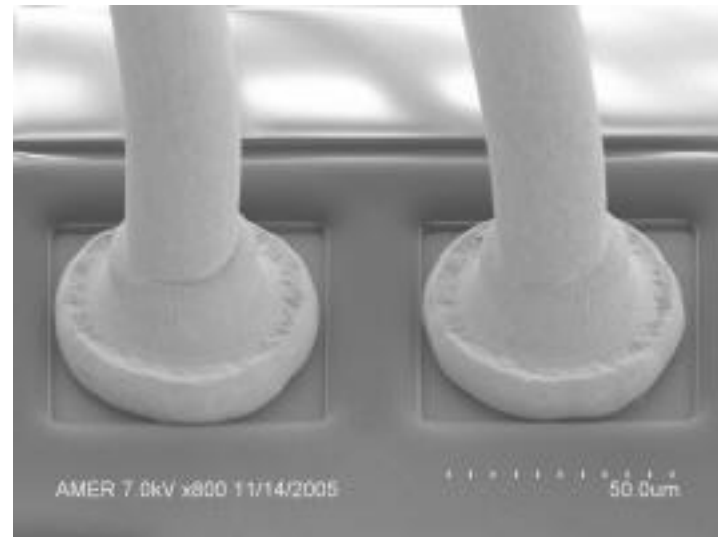
- Connect pads to chip with Au or Al wires

Wedge Bond

Ball Bond



10%

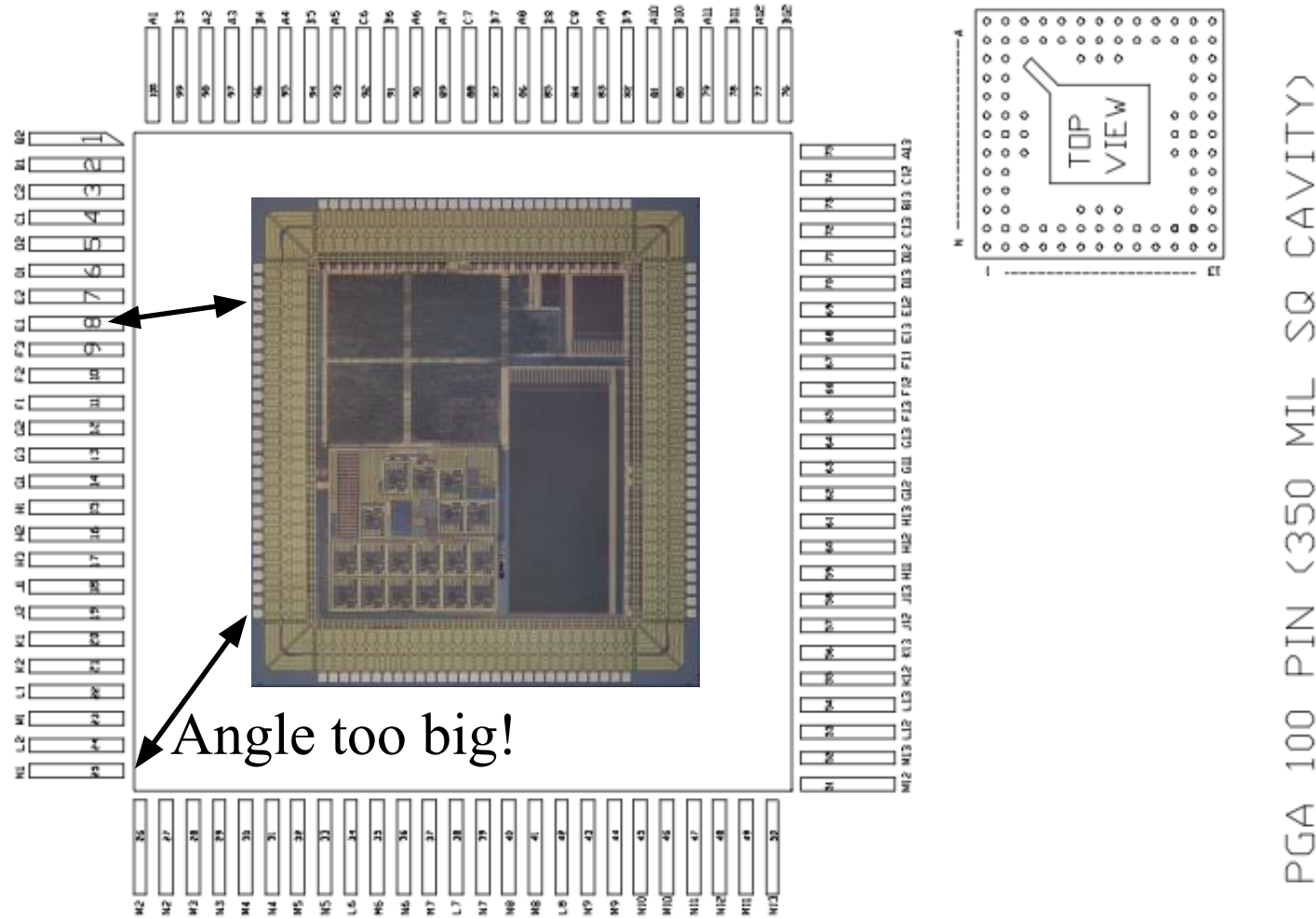


90%

From [klabs.org](http://klabs.org)



# PGA 100 Bond Diagram



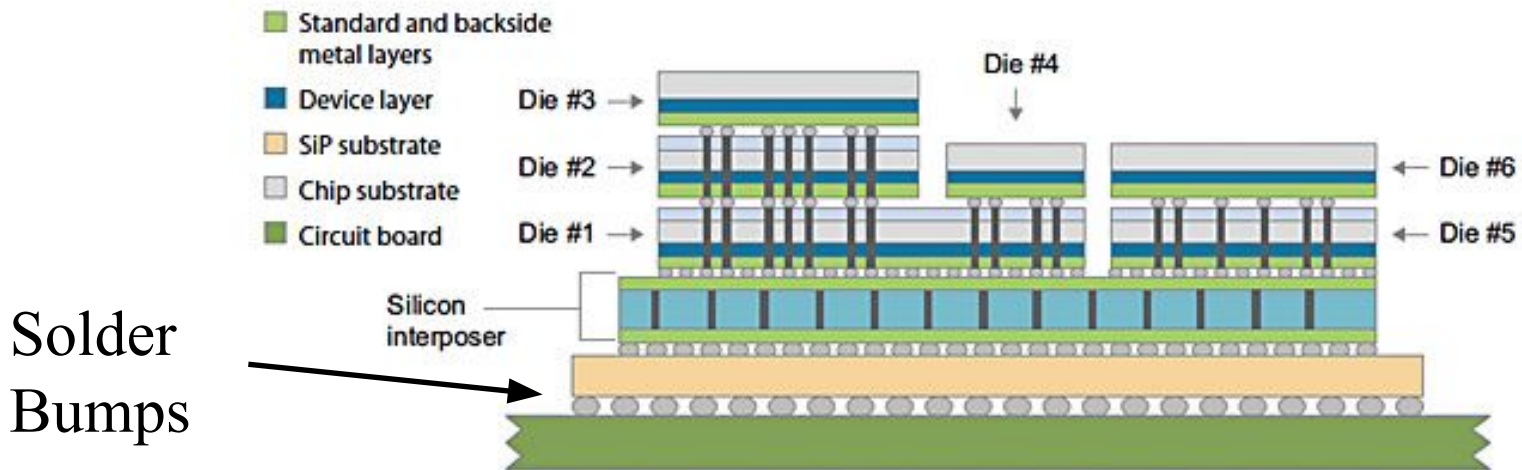
Limit on bond wire length too.

1 mil = 25.4 microns



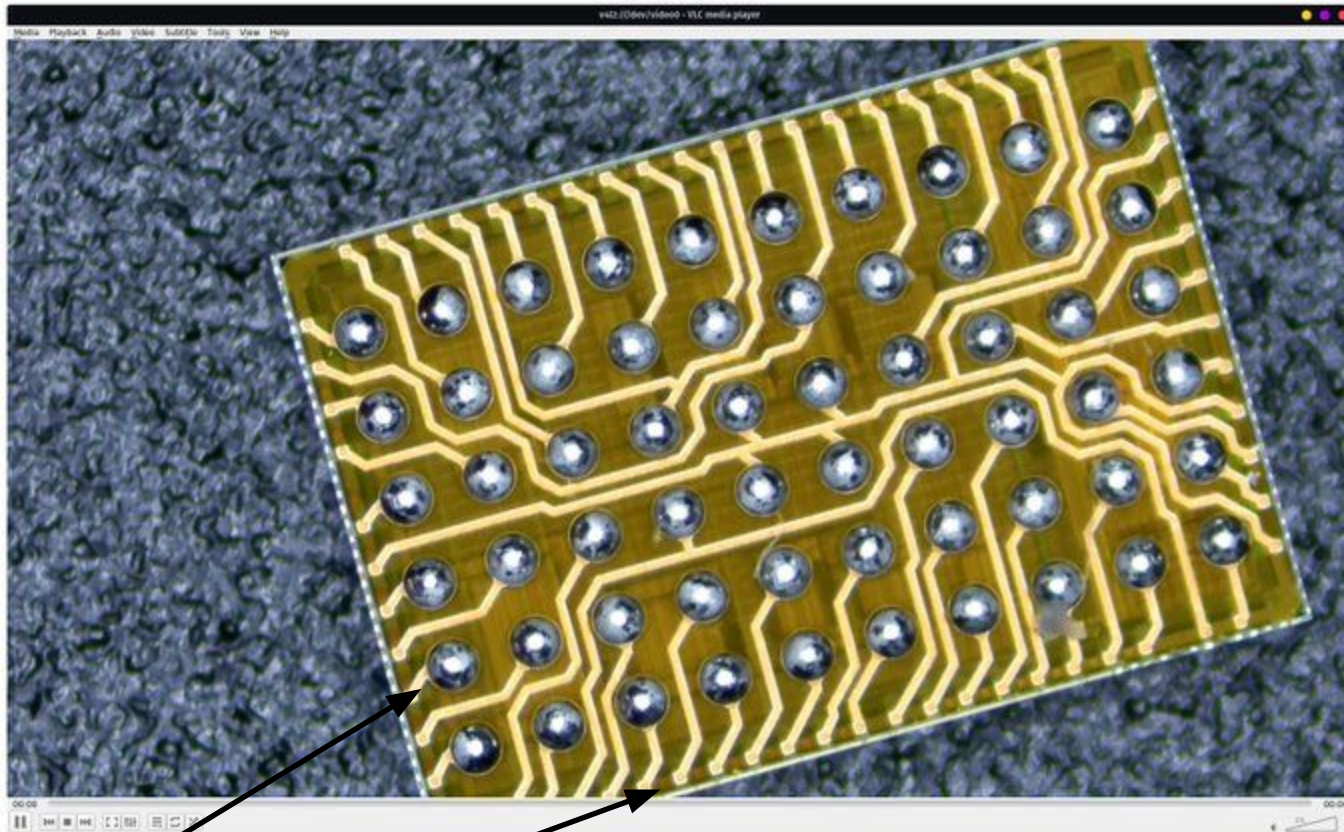
# Flip Chip

- Flip-chip places connections across surface of die rather than around periphery (allows 300-400 IO)
  - Top level metal pads covered with solder balls
  - Chip flips upside down
  - Carefully aligned to package (done blind!)
  - Heated to melt balls
  - Also called C4 (Controlled Collapse Chip Connection)





# OpenRAM MPW2 Test Chip

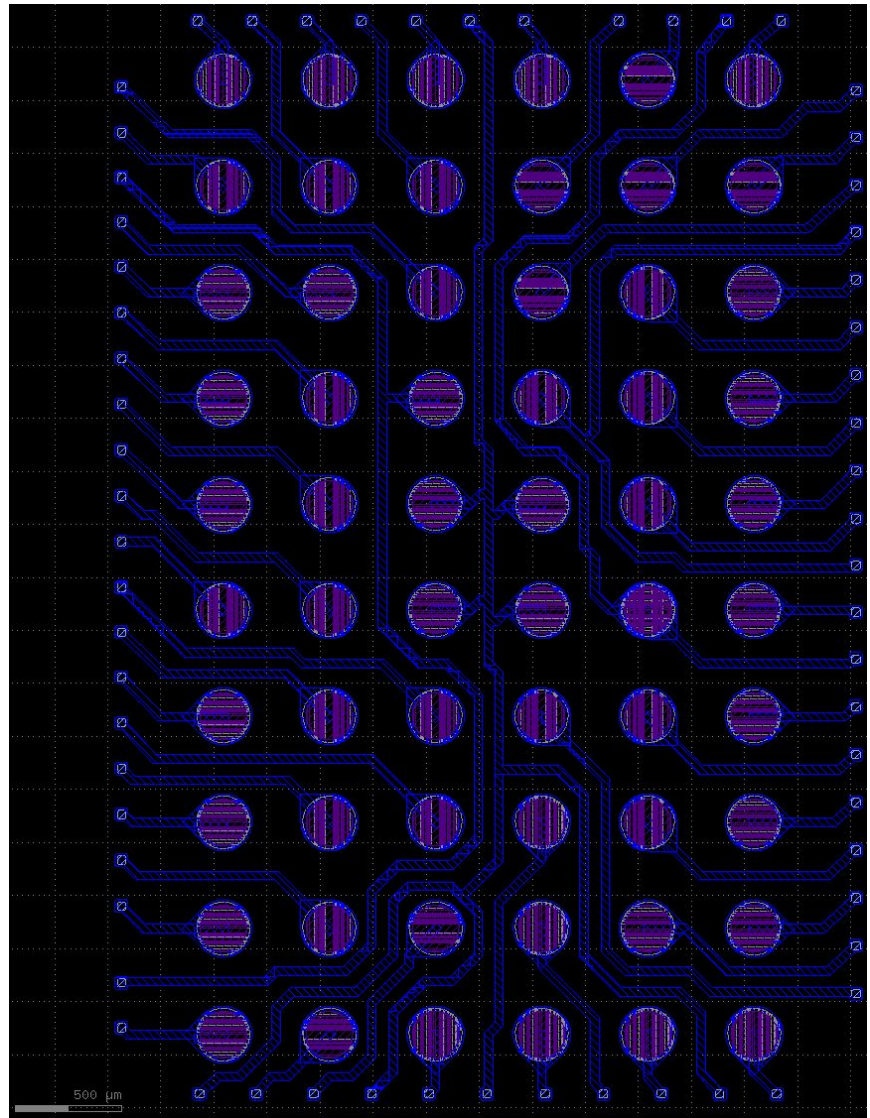
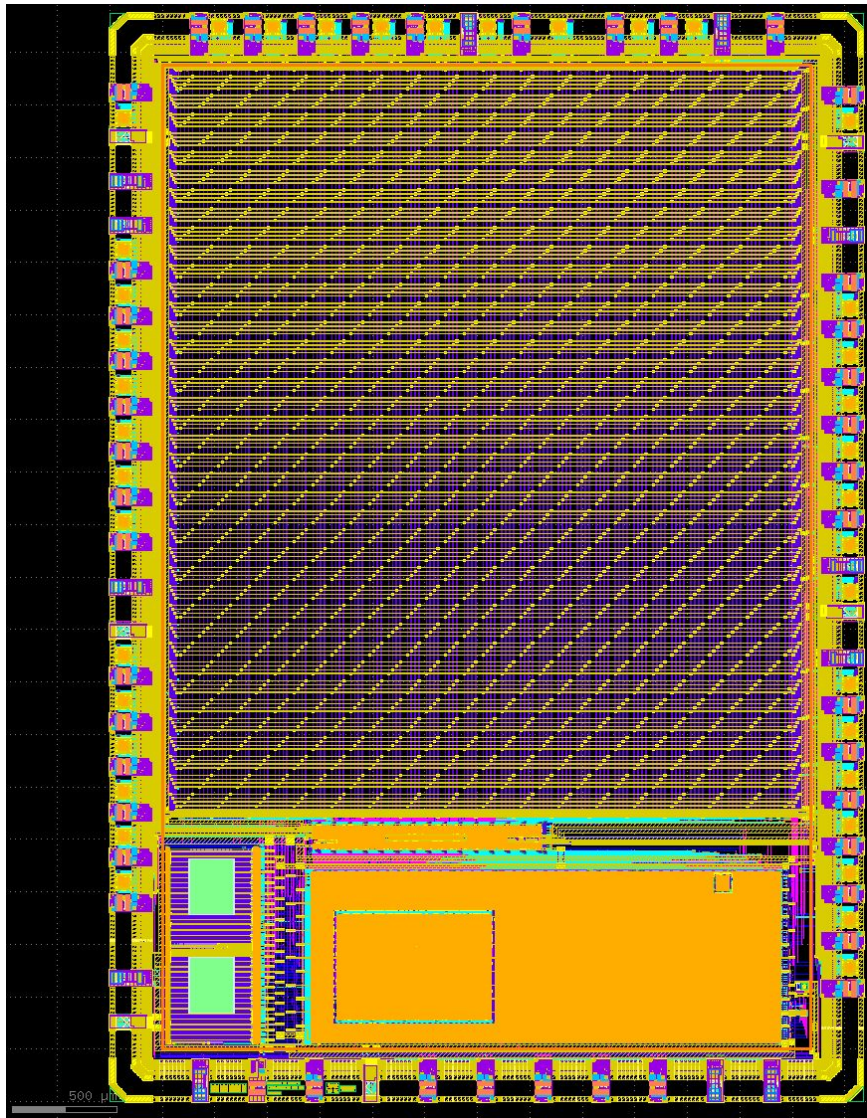


Solder  
Bumps

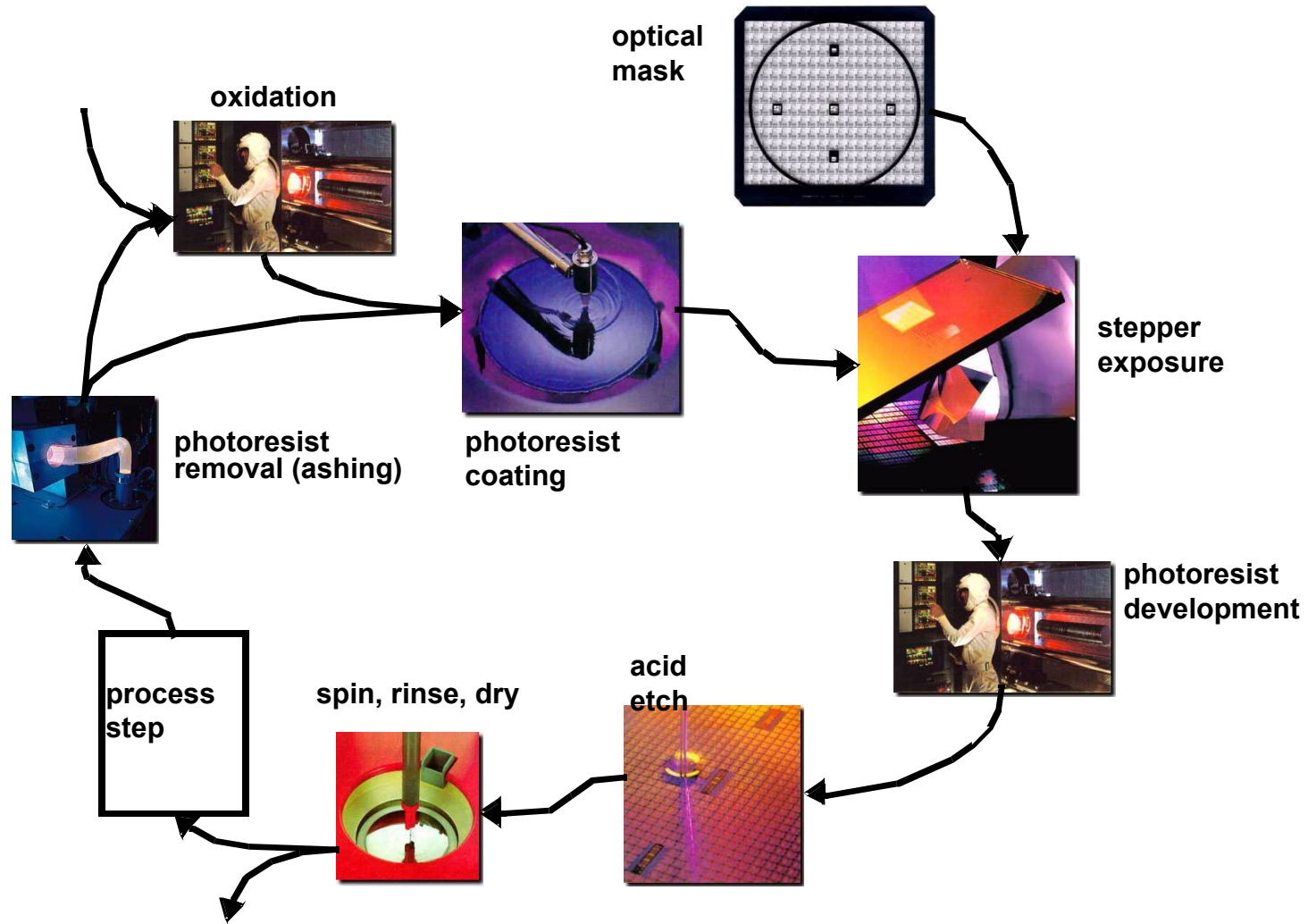
Redistribution Layer  
(RDL)



# Bump Bond Overlap Mask



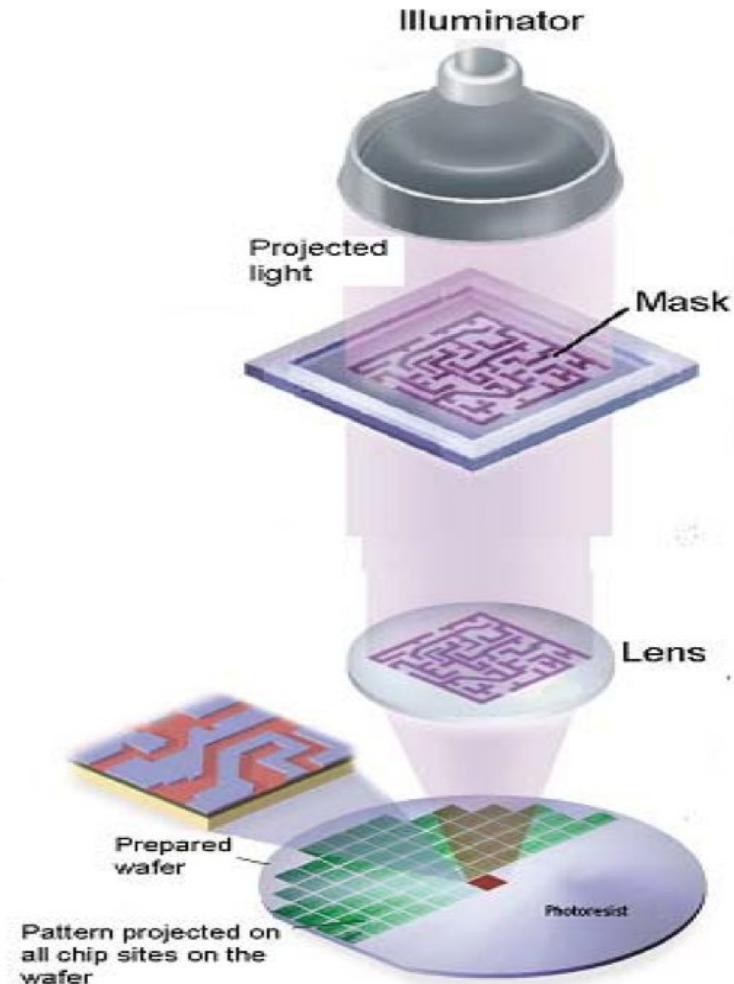
# Photolithographic Process





# Photolithography

- UV is 192nm, but our dimensions are less than this
- Samsung/TSMC EUV (13.5nm) for 5nm

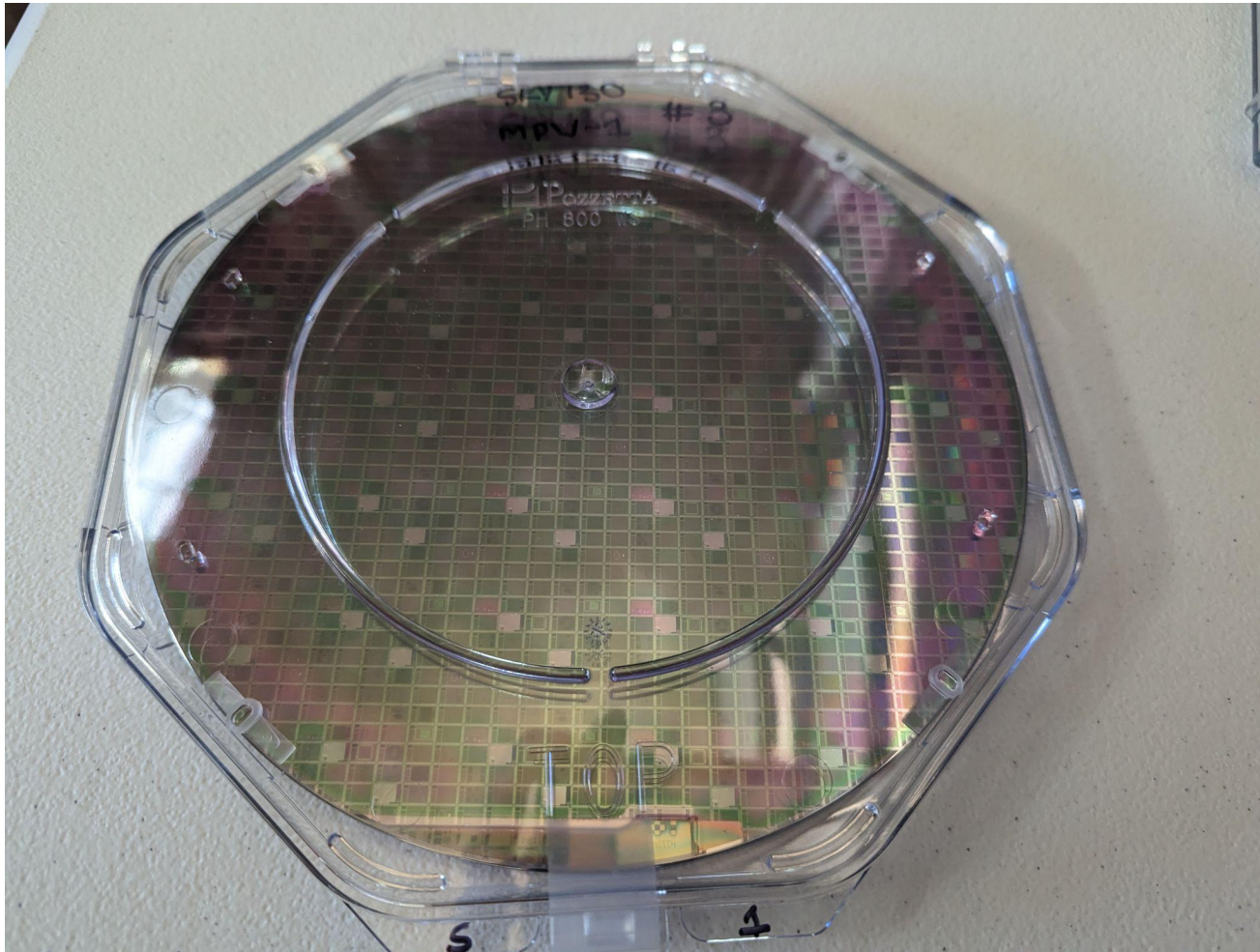


# Sky130 MPW-1 Metal 1 Mask



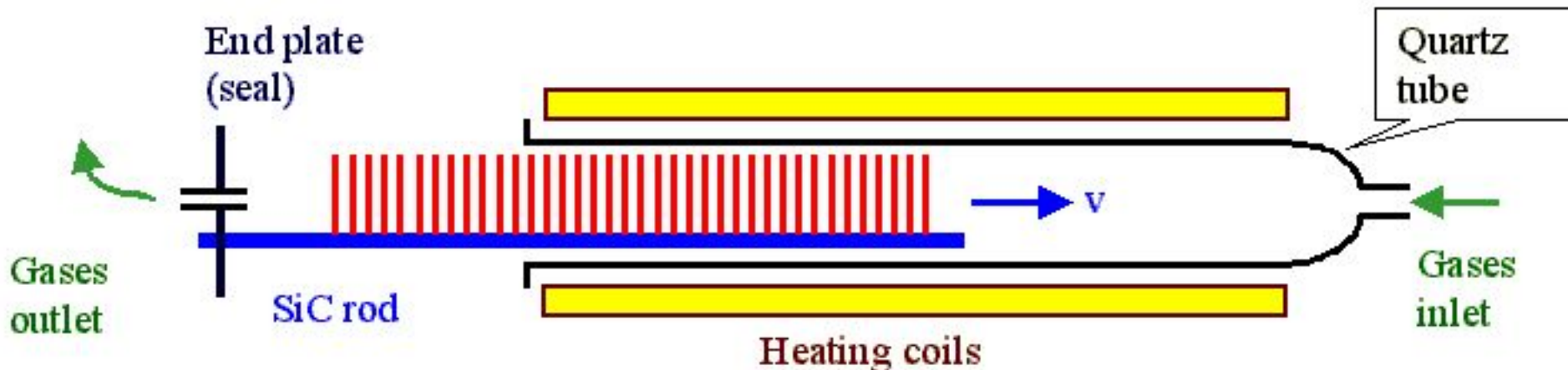
# Skywater 130nm Wafer

~8 inch wafer (200mm)



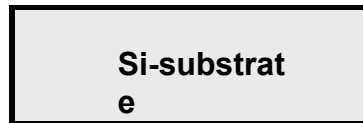
# Oxidation

- Mix oxygen and hydrogen
- 1000C
- Turns Si to SiO<sub>2</sub>
- Slower growth yields finer/better oxide (e.g. gate)





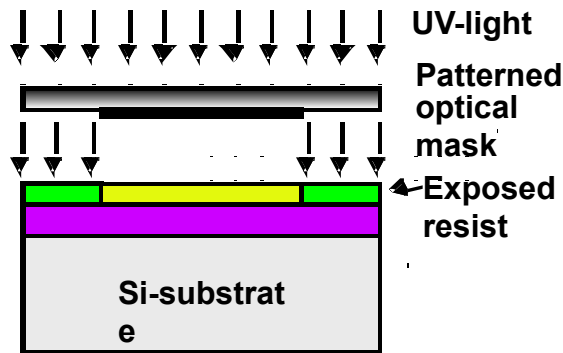
# Patterning of SiO<sub>2</sub>



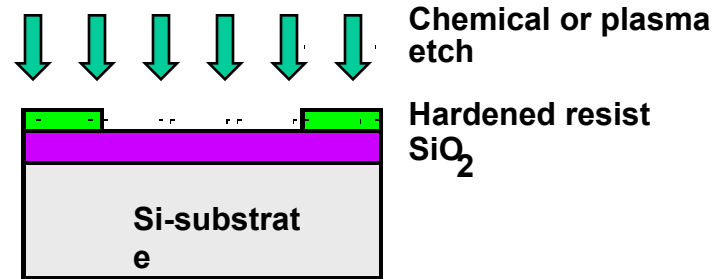
(a) Silicon base material



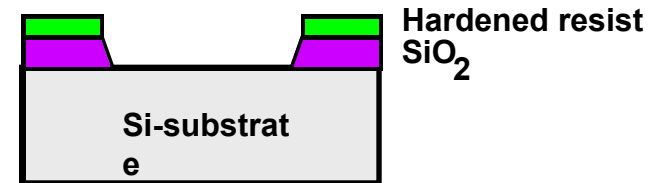
(b) After oxidation and deposition of negative photoresist



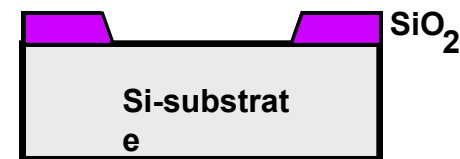
(c) Stepper exposure



(d) After development and etching of resist, chemical or plasma etch of SiO<sub>2</sub>



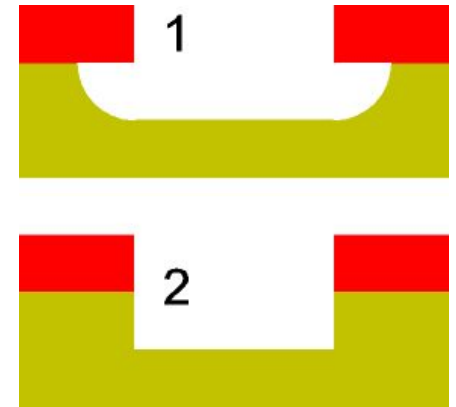
(e) After etching



(f) Final result after removal of resist

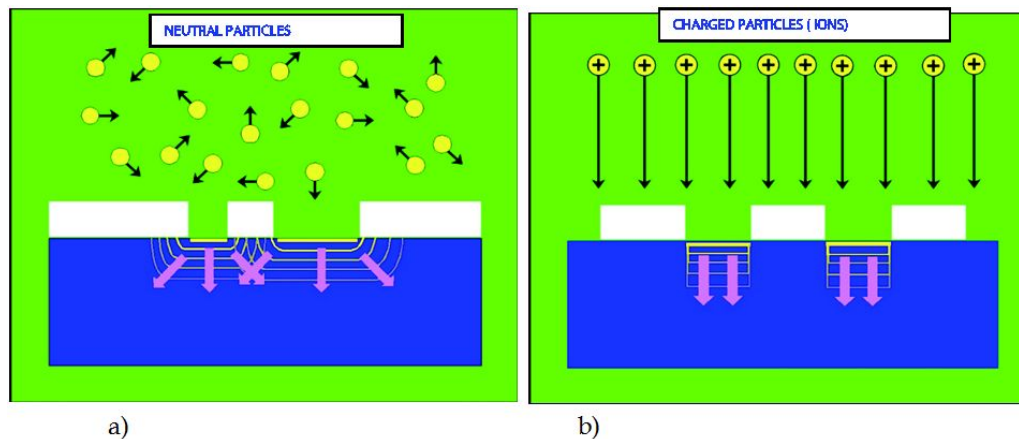
# Etching

- Used to form patterns
- Wet Etching
  - Acid or base solution
  - Isotropic (all directions) etch
- Dry (Plasma) Etching
  - Negative charge wafer, 100C, vacuum
  - Fill with positive plasma (Nitrogen, Chlorine, Boron trichloride)
  - Anisotropic “sandblasting” in one direction



# Implantation

- Change dopant concentration
  - P-type or n-type or p<sup>+</sup>-type or n<sup>+</sup>-type
- Diffusion (slow)
  - High temp 900-1100C
  - Greatest concentration at surface
- Ion (fast)
  - Shoots beam at surface
  - Depth depends on speed
  - Must anneal the material to fix damage



# Deposition

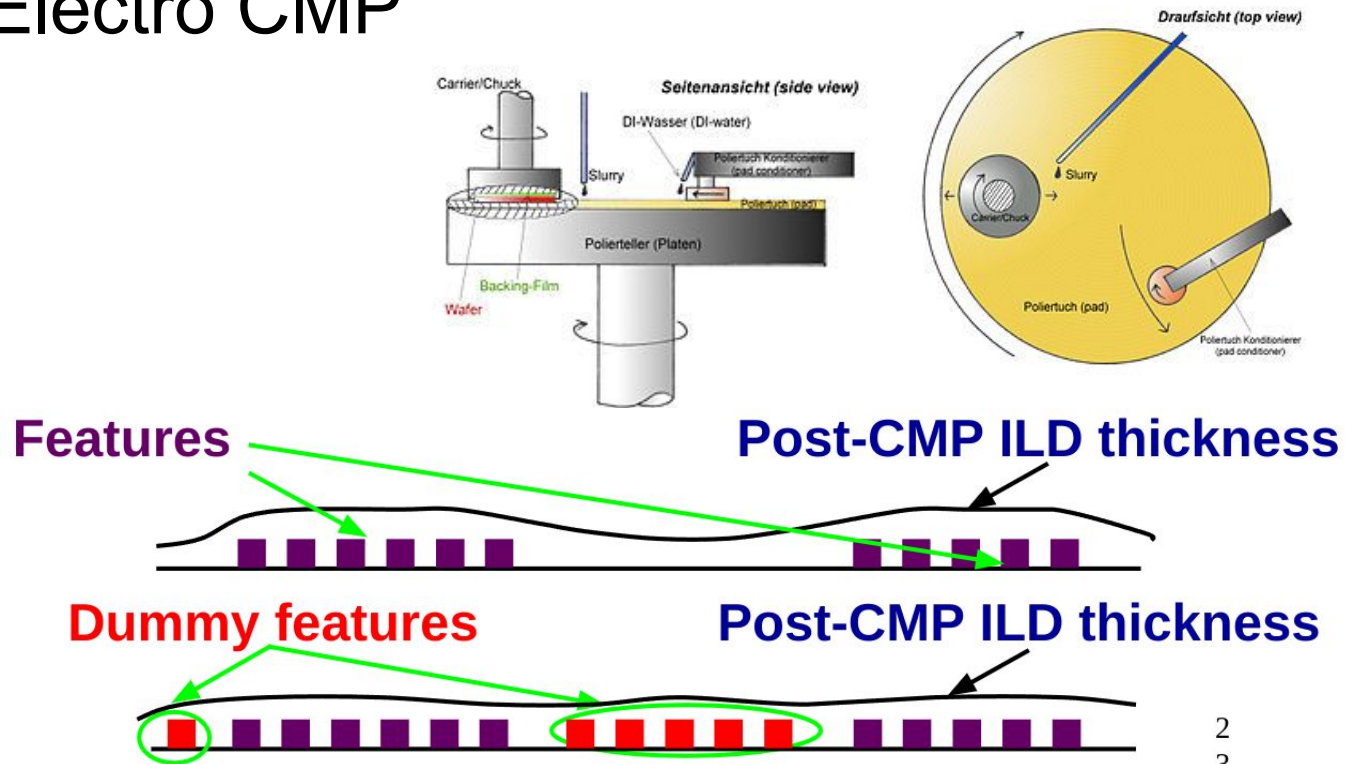
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- Chemical Vapor Deposition (CVD)
  - Silicon Nitride ( $\text{Si}_3\text{N}_4$ )
  - Gas-phase reaction at 850C
  - Polysilicon
- Sputtering
  - Aluminum
- Physical Vapor Deposition (PVD)
  - Copper



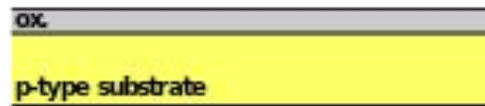
# Planarization

- Chemical Mechanical Polishing (CMP)
  - Slurry liquid with abrasive like silica
  - Flexible pad grinds a layer off
  - Electro CMP

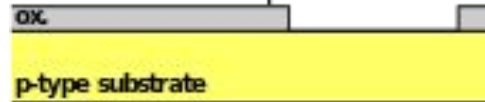


# Typical CMOS Process

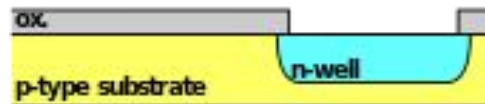
1. Grow field oxide



2. Etch oxide for pMOSFET



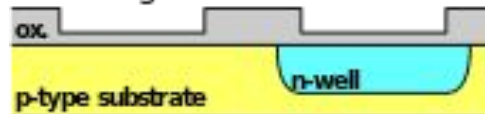
3. Diffuse n-well



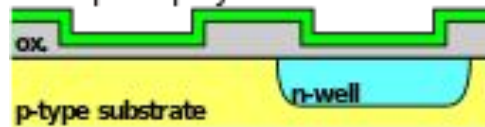
4. Etch oxide for nMOSFET



5. Grow gate oxide



6. Deposit polysilicon



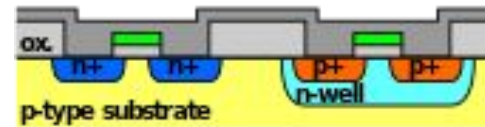
7. Etch polysilicon and oxide



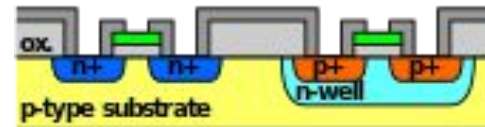
8. Implant sources and drains



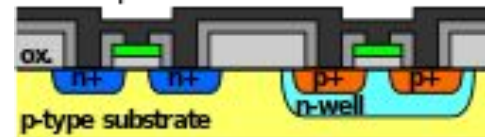
9. Grow nitride



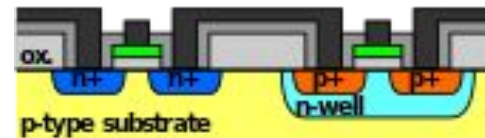
10. Etch nitride



11. Deposit metal

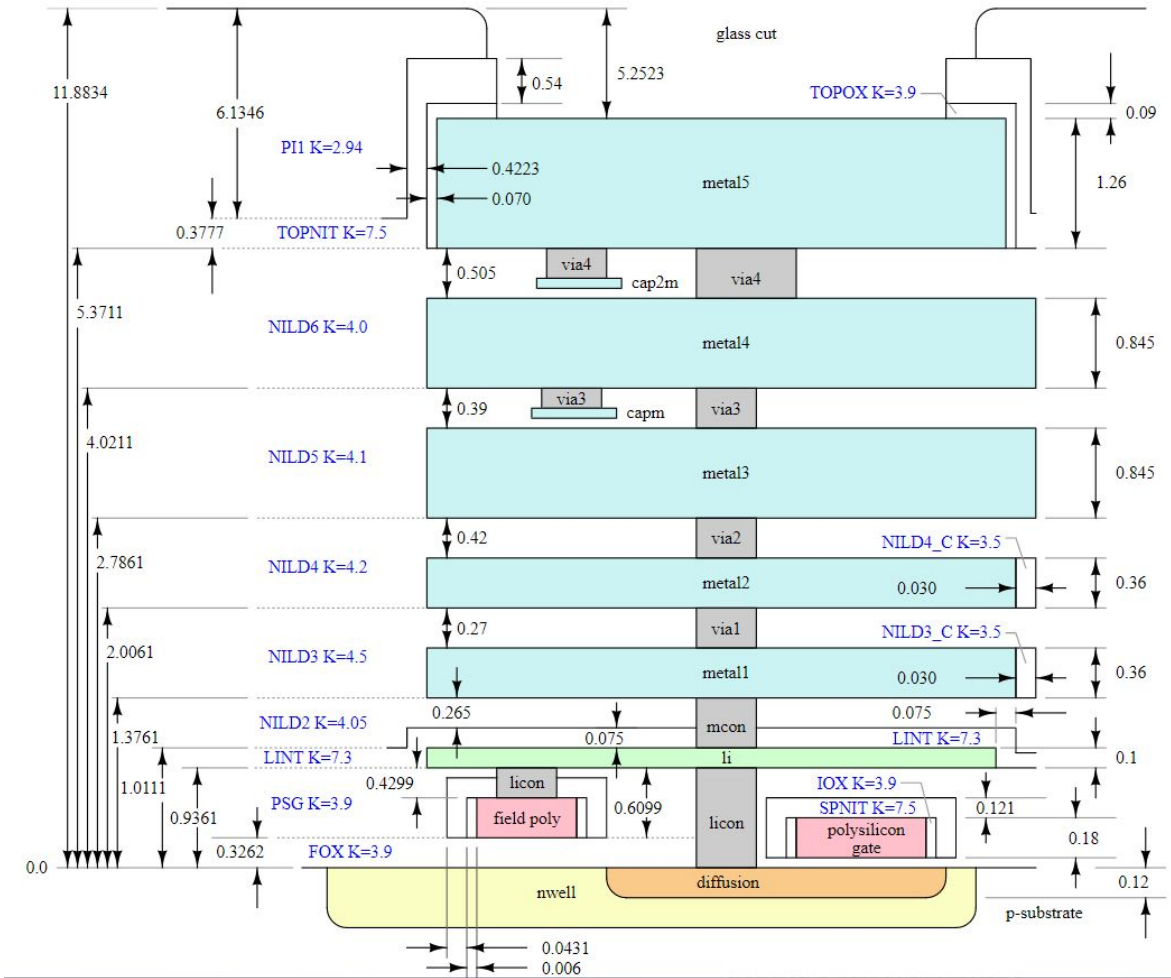


12. Etch metal



# Sky130 Layers

(Diagram not to scale!)



## Layers

	prBoundary.boundary - 235/4
	pwell.pin - 122/16
	pwell.label - 64/59
	nwell.drawing - 64/20
	nwell.pin - 64/16
	nwell.label - 64/5
	dnwell.drawing - 64/18
	diff.drawing - 65/20
	tap.drawing - 65/44
	psdm.drawing - 94/20
	nsdm.drawing - 93/44
	poly.drawing - 66/20
	poly.pin - 66/16
	poly.label - 66/5
	poly.model - 66/83
	hvtp.drawing - 78/44
	licon1.drawing - 66/44
	npc.drawing - 95/20
	li1.drawing - 67/20
	mcon.drawing - 67/44
	met1.drawing - 68/20
	met1.pin - 68/5
	met1.label - 68/16
	via.drawing - 68/44
	met2.drawing - 69/20
	met2.pin - 69/16
	met2.label - 69/5
	ncm.drawing - 92/44



# Sky130 Layers vs Masks

## Layers





























	<b>prBoundary</b> .boundary - 235/4
	<b>pwell</b> .pin - 122/16
	<b>pwell</b> .label - 64/59
	<b>nwell</b> .drawing - 64/20
	<b>nwell</b> .pin - 64/16
	<b>nwell</b> .label - 64/5
	<b>dnwell</b> .drawing - 64/18
	<b>diff</b> .drawing - 65/20
	<b>tap</b> .drawing - 65/44
	<b>psdm</b> .drawing - 94/20
	<b>nsdm</b> .drawing - 93/44
	<b>poly</b> .drawing - 66/20
	<b>poly</b> .pin - 66/16
	<b>poly</b> .label - 66/5
	<b>poly</b> .model - 66/83
	<b>hvtp</b> .drawing - 78/44
	<b>licon1</b> .drawing - 66/44
	<b>npc</b> .drawing - 95/20
	<b>li1</b> .drawing - 67/20
	<b>mcon</b> .drawing - 67/44
	<b>met1</b> .drawing - 68/20
	<b>met1</b> .pin - 68/5
	<b>met1</b> .label - 68/16
	<b>via</b> .drawing - 68/44
	<b>met2</b> .drawing - 69/20
	<b>met2</b> .pin - 69/16
	<b>met2</b> .label - 69/5
	<b>ncm</b> .drawing - 92/44

Table 1 Table - Masks

Mask	Acronym	Used in SKY130
Field Oxide	FOM	X
Deep N-Well	DNM	X
P-Well Block Mask	PWBM	
P-Well Drain Extended	PWDEM	
N-Well*	NWM	X
High Vt PCh*	HVTPM	X
Low Vt Nch*	LVTNM	X
HLow VT PCh Radio*	HVTRM	X
N-Core Implant	NCM	
Tunnel Mask	TUNM	X
ONO Mask	ONOM	X
Low Voltage Oxide	LVOM	X
Resistor Protect	RPM	X
Poly 1	P1M	X
N-tip Implant	NTM	X
High Volt. N-tip	HVNTM	X
Lightly Doped N-tip	LDNTM	X
Nitride Poly Cut	NPCM	X
P+ Implant	PSDM	X
N+ Implant	NSDM	X
Local Intr. Cont.1	LICM1	X
Local Intrcnct 1	LI1M	X
Contact	CTM1	X
Open Frame Mask	OFM	

Metal 1	MM1	X
Via	VIM	X
Capacitor MiM	CAPM	
Metal 2	MM2	X
Via 2-TNV	VIM2	
Via 2-S8TM	VIM2	
Via 2-PLM	VIM2	X
Metal 3-TLM	MM3	
Metal 3-S8TM	MM3	
Metal 3-PLM	MM3	X
Pad Via	VIPDM	
Via3-PLM	VIM3	X
Inductor-TLM	INDM	
Metal 4	MM4	X
Via4	VIM4	X
Metal 5	MM5	X
Nitride Seal Mask	NSM	X
Pad (scribe protect)	PDM	X
Pad (scribe unprotect)	PDM	
Polyimide	PMM	
Polyimide_ExtFab	PMM[E]	
Pad&Polyimide_ExtFab	PDMM[E]	
DECA PBO	PBO	X
Cu Inductor/Redist.	CU1M	X
Polyimide 2 (2)	PMM2	X
Under Bump Metal	UBM	
Bumps	BUMP	

# Next Time

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- Layout (for HW1!)

