CSE 122/222A
Lecture 01: Introduction

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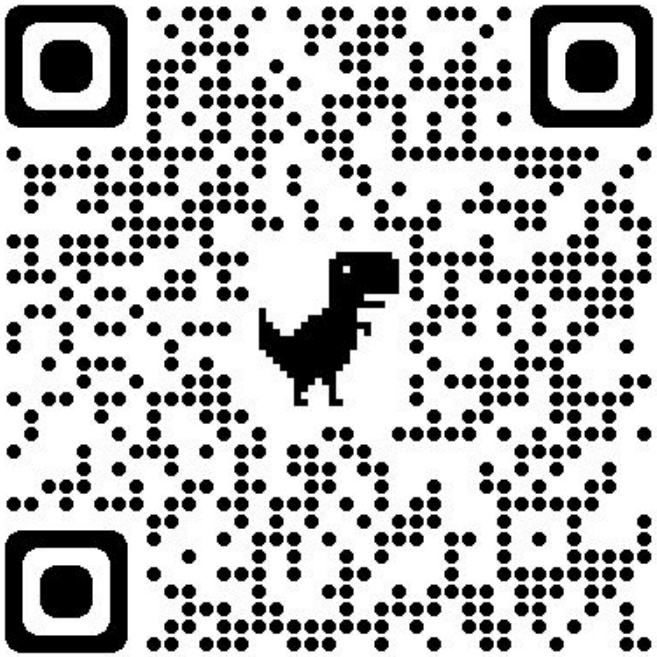
Today's Lecture

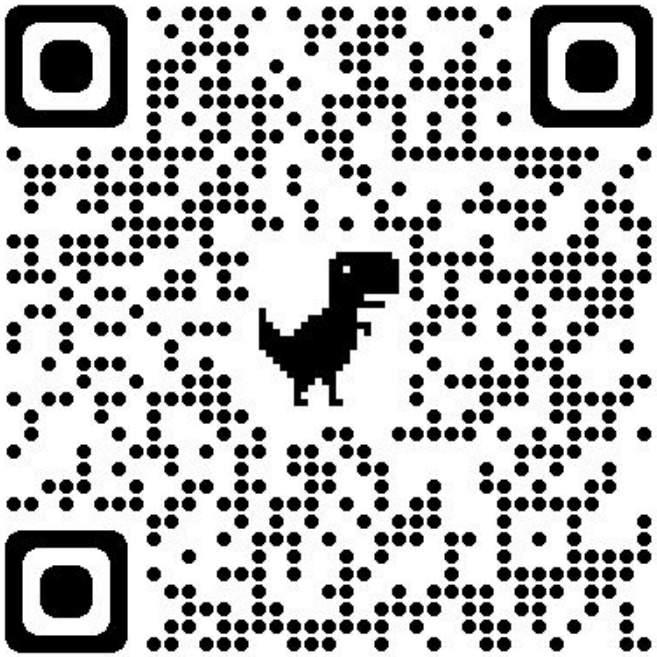
- Why should we still learn VLSI?
- High-level (digital) design flows



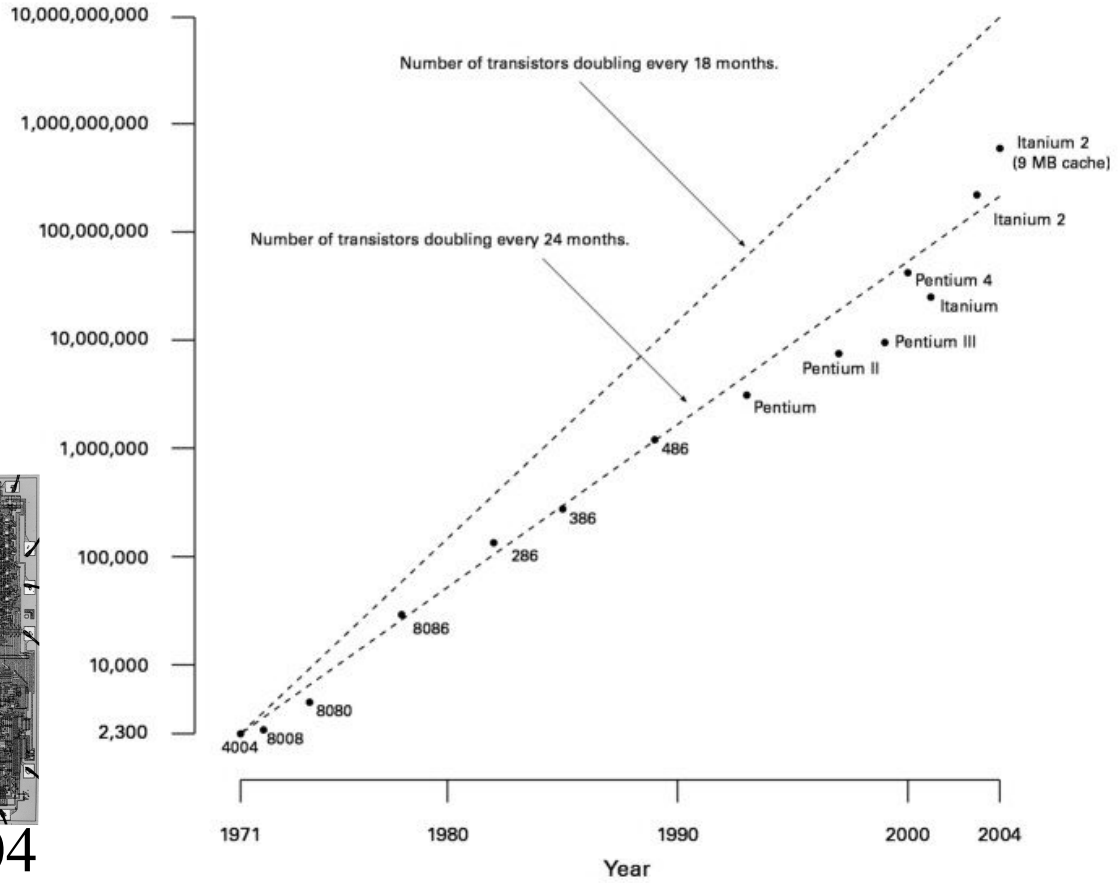
Syllabus

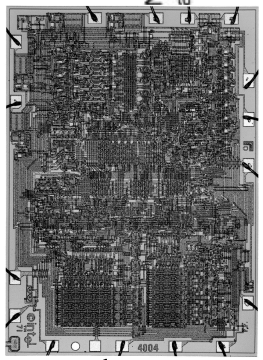
- https://vlsida.github.io/cse122-222a-s23/syllabus.html

•This is a project class!

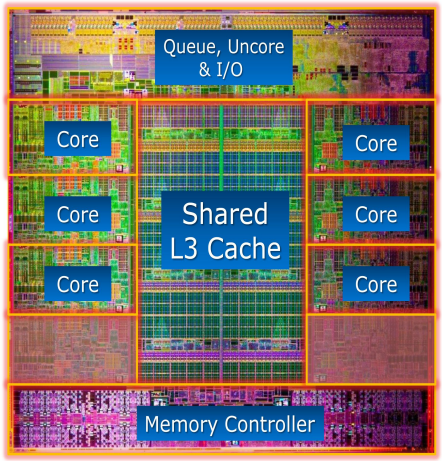


Moore's Law is DEAD?





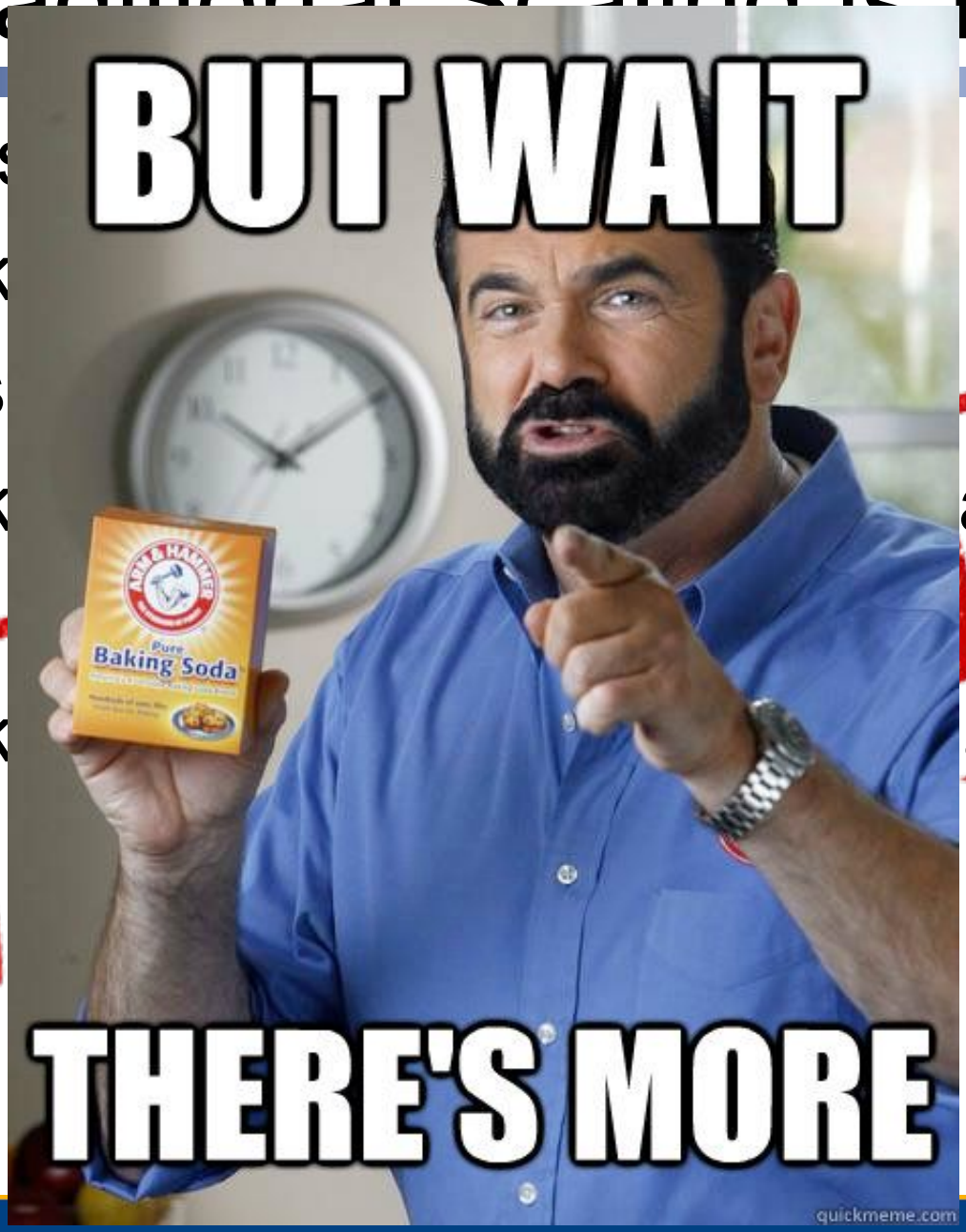
Intel 4004
2300 transistors

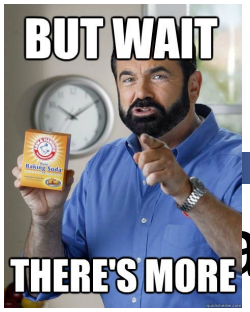


Intel Core i7
~1.4B transistors

Traditional Scaling is Dead

- Power s
  - Stuck
- Transis
  - Stuck ater)
- Adding
  - Stuck ater)

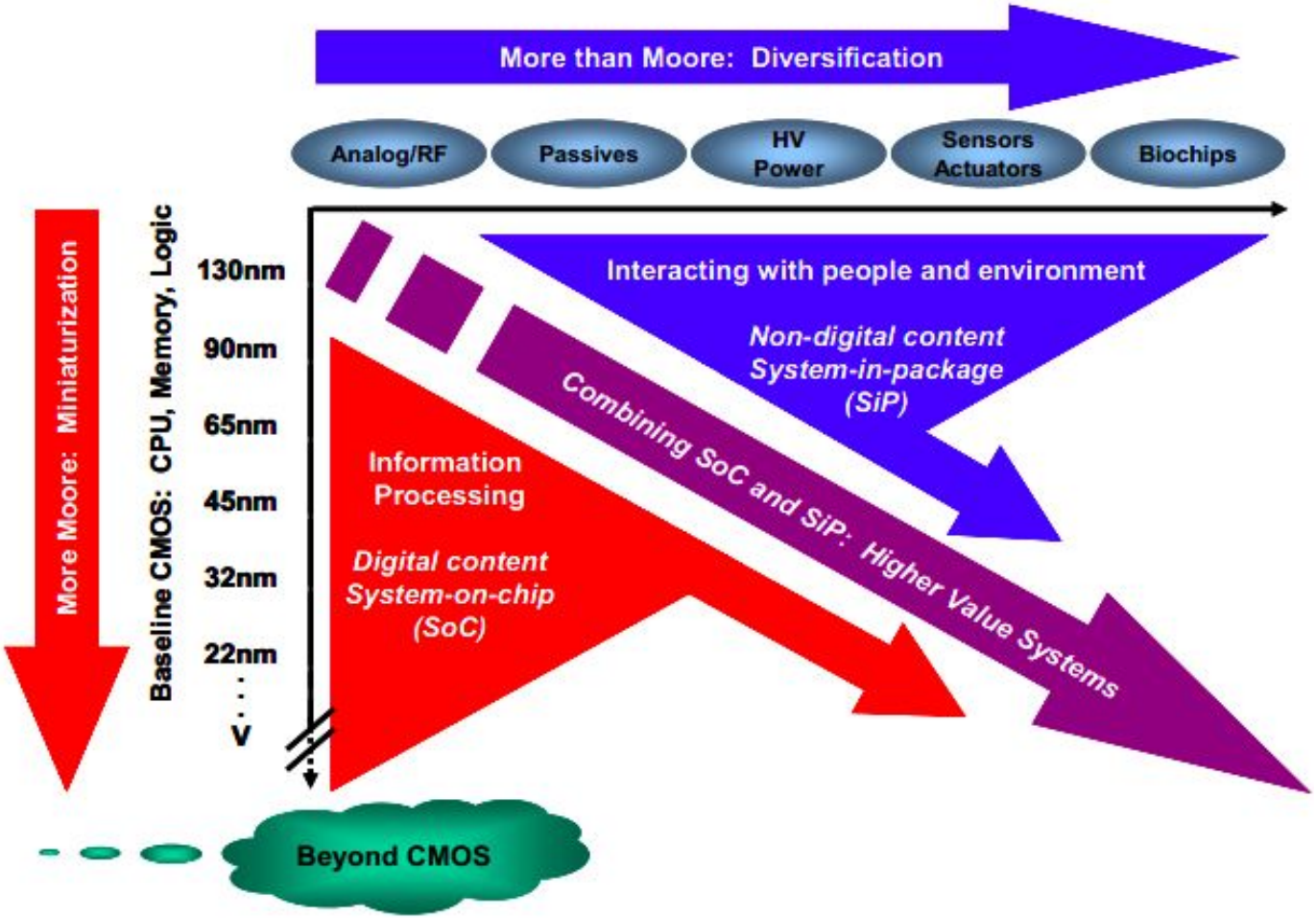




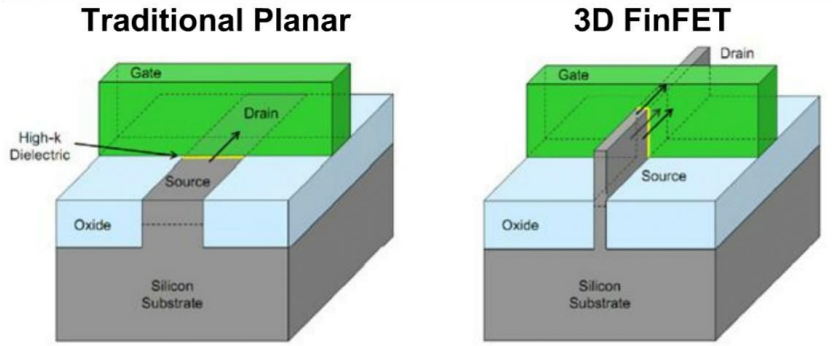
But wait… there's more.

- at else is in a "system"?
  - Storage, displays, analog, sensors…
  - Integrate other parts on-chip! (maybe not displays…)
- Why do we assume chips are flat?
  - Stack vertically? Yes, possibly!

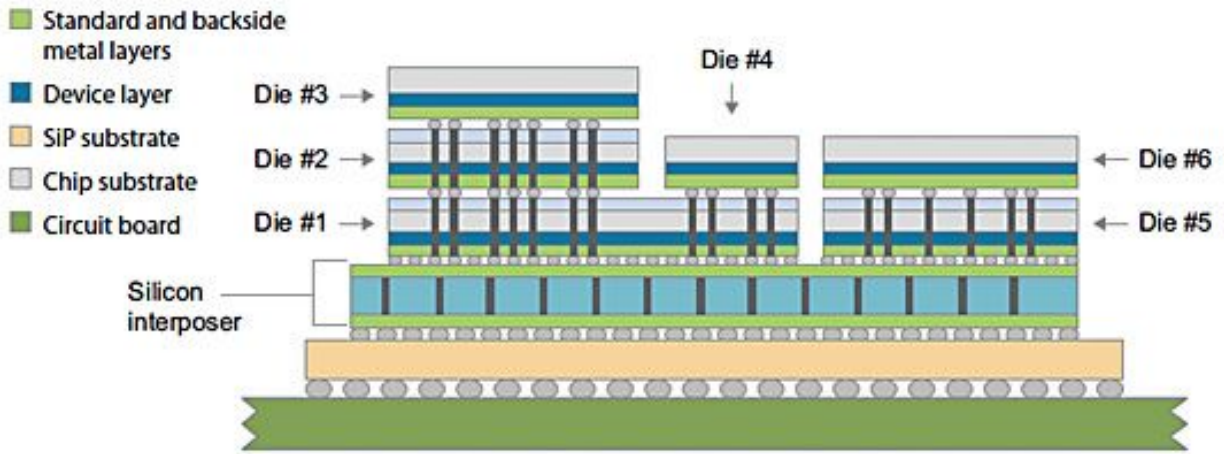
More than Moore



More Moore and More than Moore

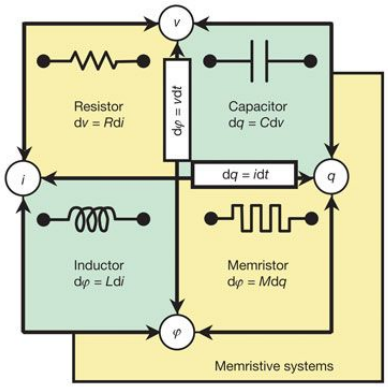


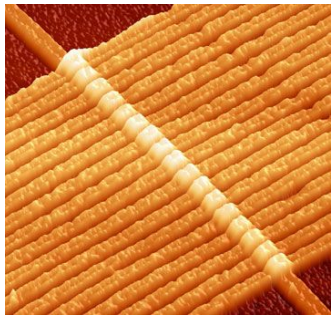
FinFETs



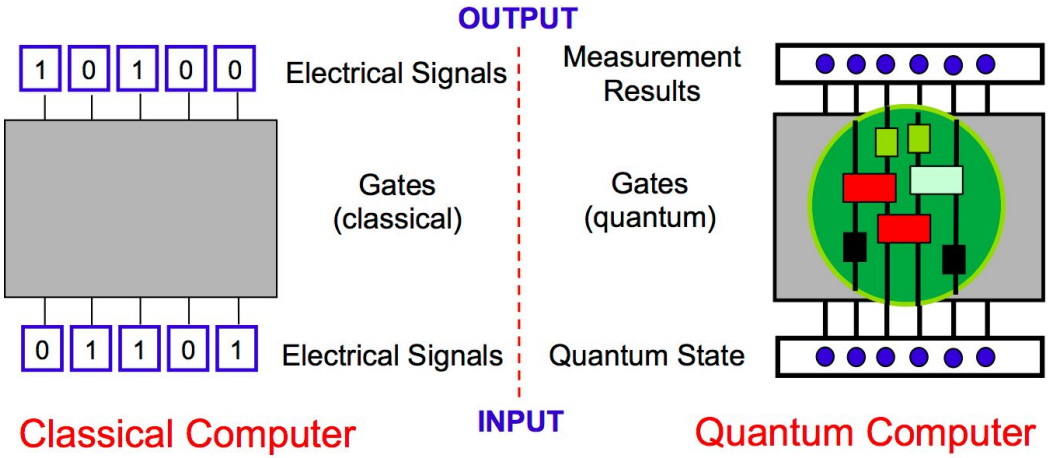
3D ICs, System-in-Package
(Face-to-Face, TSVs, etc.)

Beyond Moore

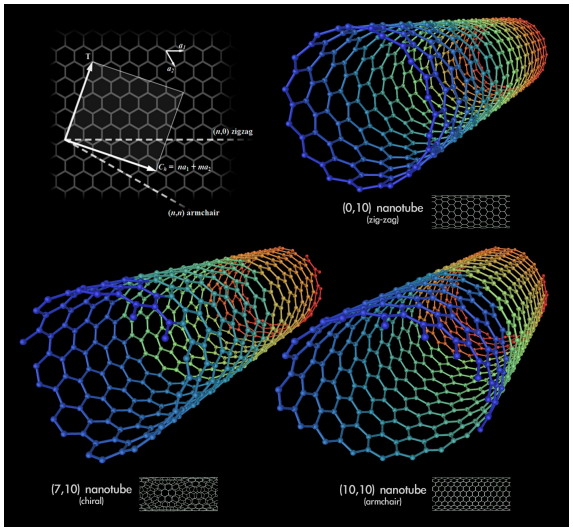




Memristors



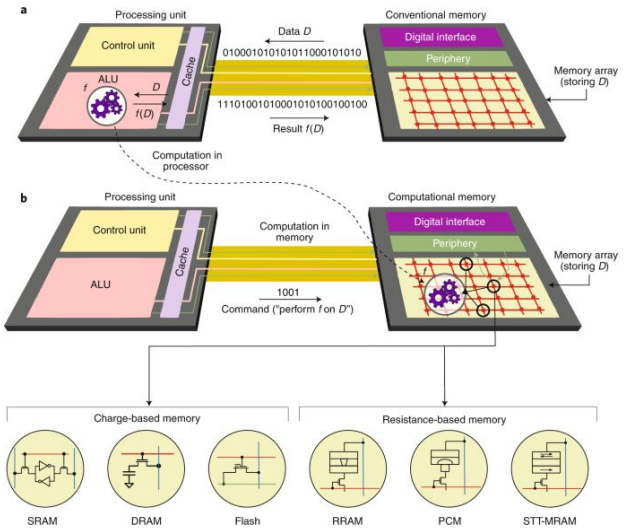
Quantum Computing



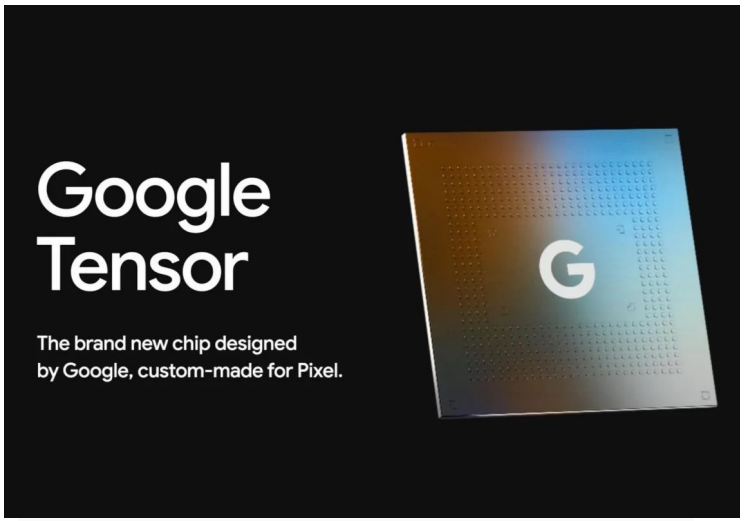
Carbon Nanotubes

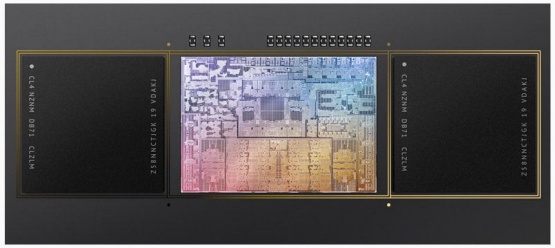
New Architectures

Compute In Memory



HODL!!





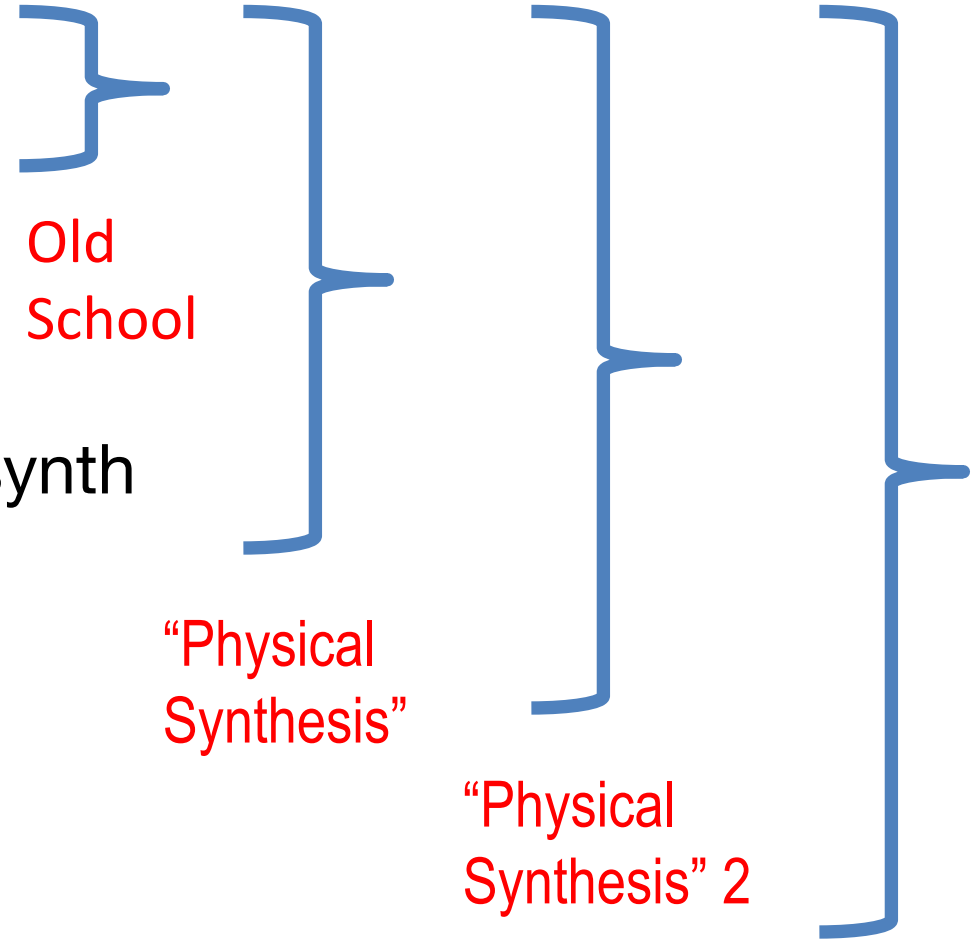
Apple M1 Neural Engine

New Abstractions

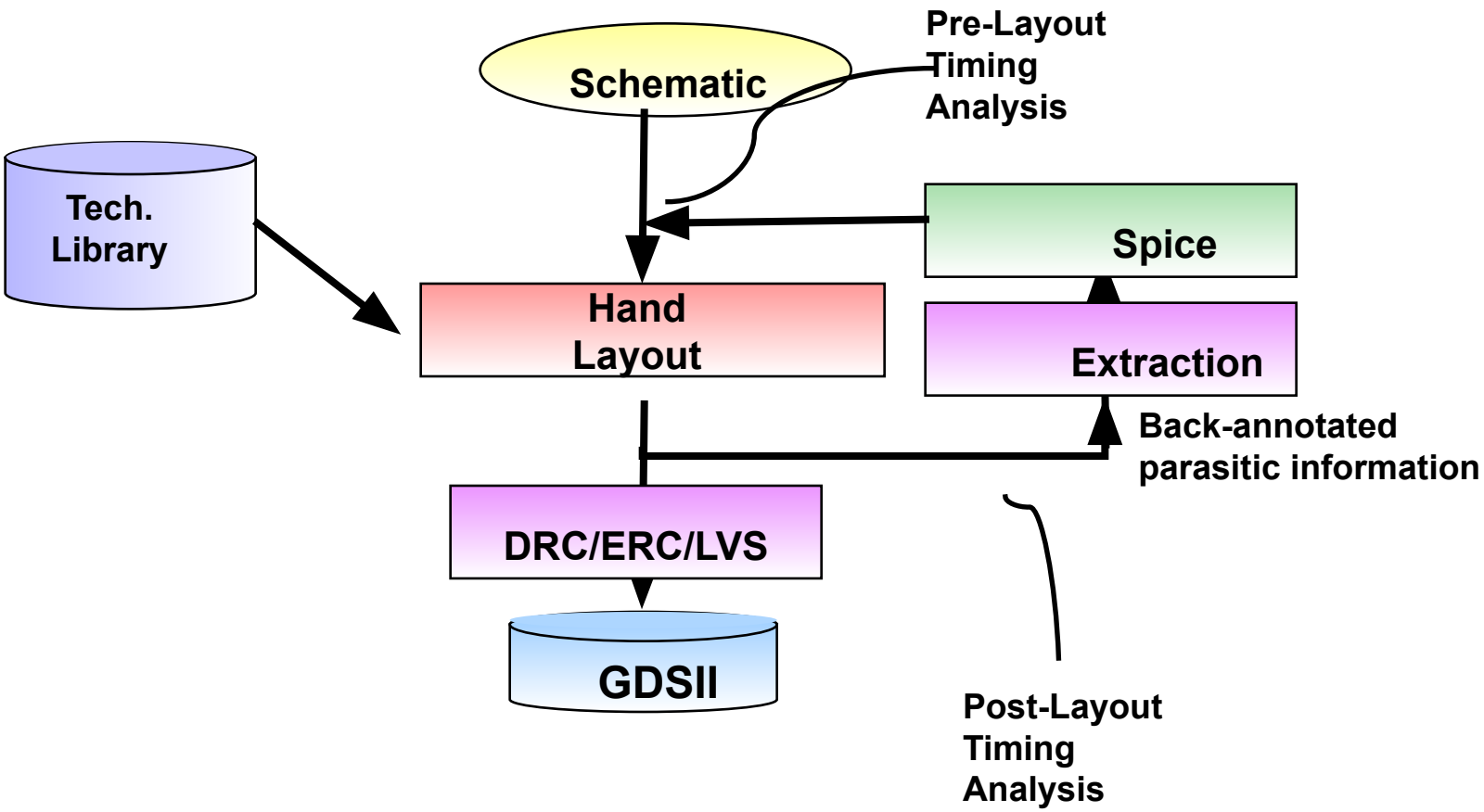
- All use Standard Cell backend
- Examples:
  - System Verilog
  - Bluespec
  - Chisel – Scala
  - PyMTL
  - PyRTL
  - Nmigen (now Amaranth HDL)
  - Silicon Compiler

Evolution of ASIC Optimization

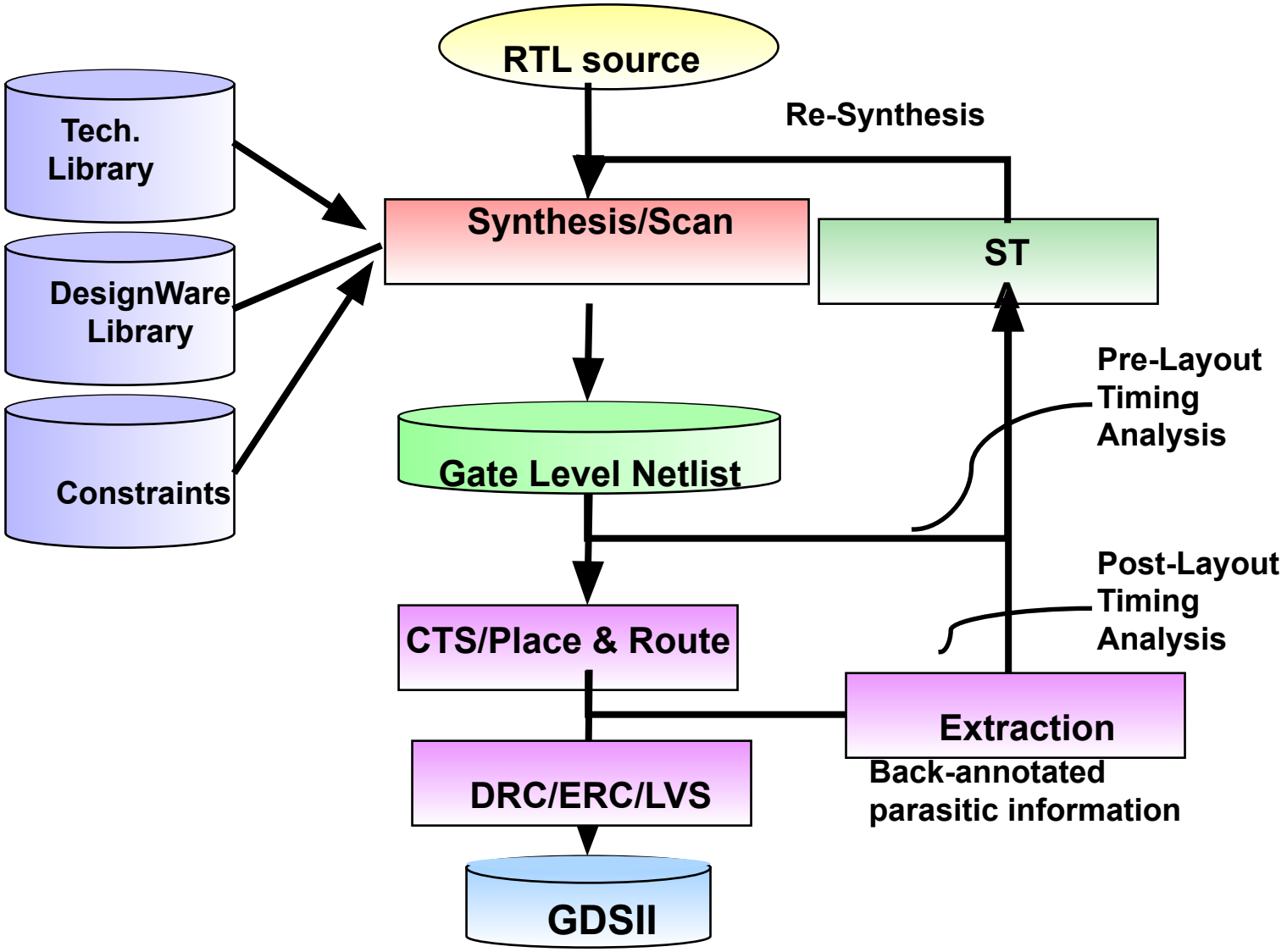
- HDL Implementation
- Synthesis
- Floorplanning
  - Power, pins, thermal
- Placement
  - Buffering, Sizing, Resynth
- Clock Synthesis
- Routing
- OPC/RET
- Yield optimization
- Sign-off/Tape-out



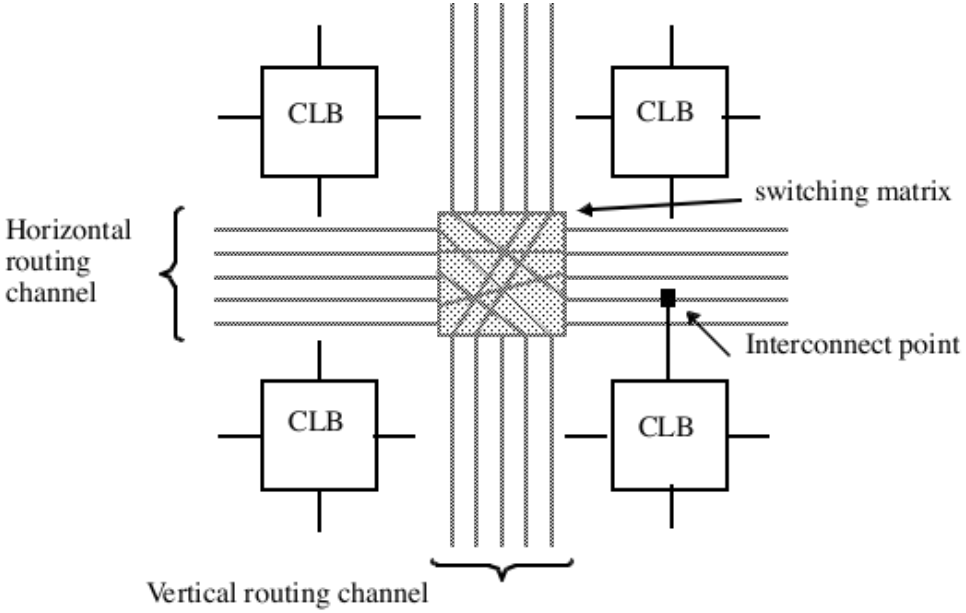
Full Custom Design Flow

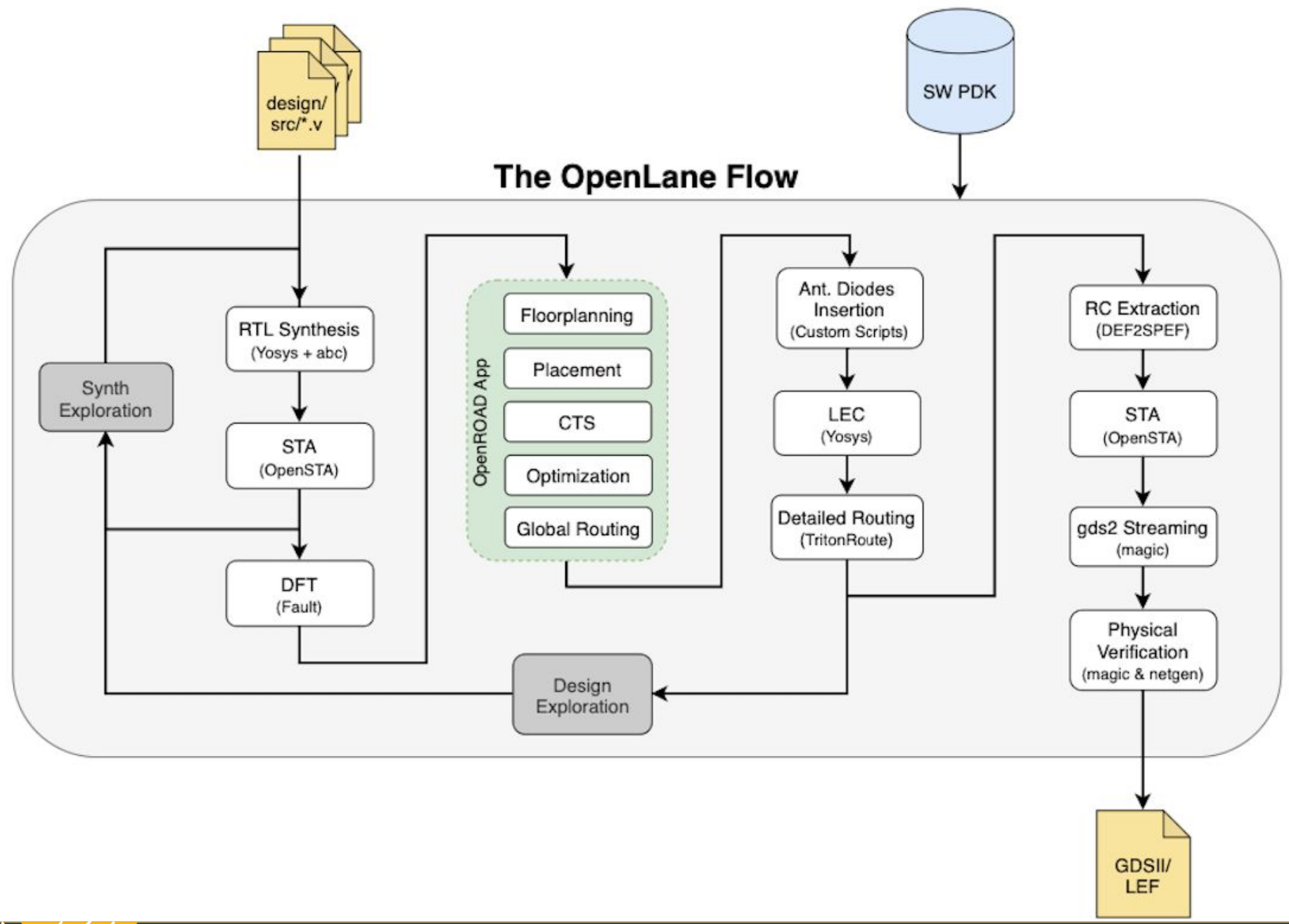


Standard Cell Design Flow

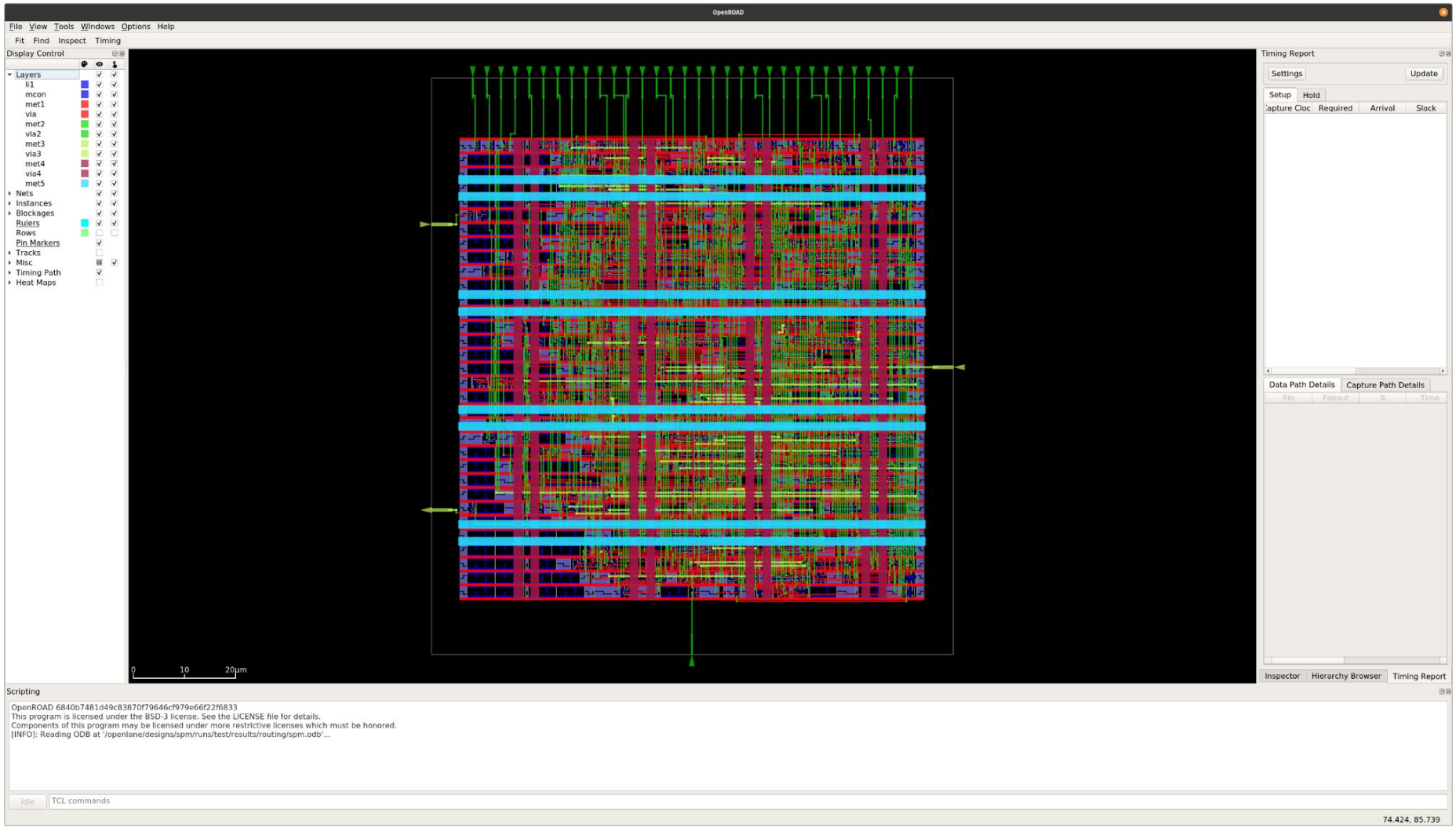


FPGA Design Flow




design/
src/*.v
SW PDK
The OpenLane Flow
Synth
Exploration
RTL Synthesis
(Yosys + abc)
STA
(OpenSTA)
DFT
(Fault)
OpenROAD App
Floorplanning
Placement
CTS
Optimization
Global Routing
Ant. Diodes
Insertion
(Custom Scripts)
LEC
(Yosys)
Detailed Routing
(TritonRoute)
RC Extraction
(DEF2SPEF)
STA
(OpenSTA)
gds2 Streaming
(magic)
Physical
Verification
(magic & netgen)
Design
Exploration
GDSII/
LEF

OpenLane


OpenROAD
File View Tools Windows Options Help
Fit Find Inspect Timing
Display Control
Layers
li1
mcon
met1
via
met2
via2
met3
via3
met4
via4
met5
Nets
Instances
Blockages
Rulers
Rows
Pin Markers
Tracks
Misc
Timing Path
Heat Maps
0 10 20µm
Timing Report
Settings
Update
Setup
Hold
Capture Cloc
Required
Arrival
Slack
Data Path Details
Capture Path Details
Pin
Fanout
Time
Inspector
Hierarchy Browser
Timing Report
Scripting
OpenROAD 6840b7481d49c83870f79646cf979e66f22f6833
This program is licensed under the BSD-3 license. See the LICENSE file for details.
Components of this program may be licensed under more restrictive licenses which must be honored.
[INFO]: Reading ODB at '/openlane/designs/spm/runs/test/results/routing/spm.odb'...
Idle
TCL commands
74.424, 85.739

High Level Course Topics

- Overview
- Fabrication
- Devices and Layout
- Cell Libraries
- Delay and Power
- Static Timing Analysis
- Floorplanning & Placement
- Clock Synthesis
- Memories
- Routing
- Chip Finishing
- Design for Manufacturing
- IOs and Packaging

What is an HDL?

- HDL: Hardware description Language
  - Introduced at the early 80s
  - Originally, for logic simulation only
  - Later, can “synthesize” a design from it directly
- Two popular families
  - Verilog: Verilog-95 (started in 85), Verilog-2001, System Verilog
  - VHDL: VHDL87, VHDL92
- Not so popular (newer)
  - System-C
  - C compilers (not so efficient)
- Europe & IBM & Government: VHDL
- USA - IBM: Verilog
- More history on verilog at http://www.asic-world.com/verilog/
- We will not cover much of this.

Synthesis

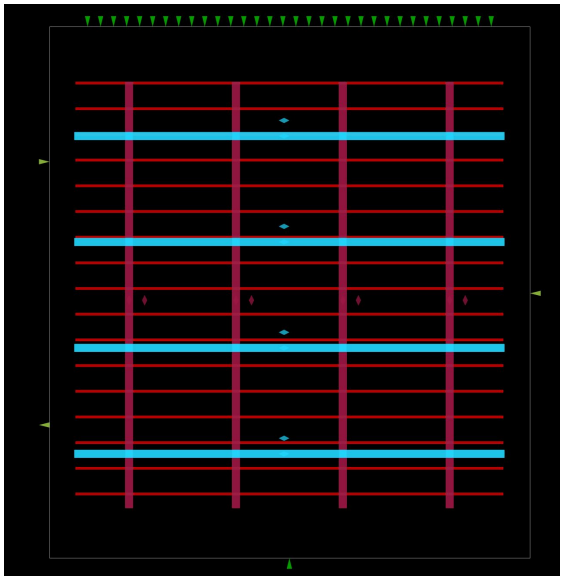
- Converts HDL to logic library gates
- High-level logic synthesis
  - Scheduling resources
  - State assignment/minimization (CMPE 100)
  - Retiming
- Logic Synthesis
  - 2-level is K-map (CMPE 100)
  - Multi-level optimization
- Common tools
  - YoSys in OpenRoad
  - Design Compiler by Synopsys
  - BooleDozer by IBM
  - Encounter RTL by Cadence
- We will not cover much of this.

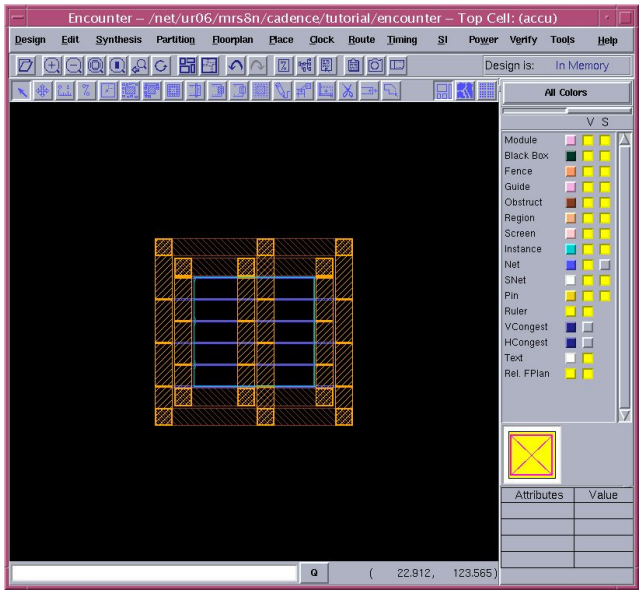
Static Timing Analysis

- Ensures setup and hold times are met
- Checks different process corners
  - Device variations
  - Interconnect variations
  - Temperatures
- Common tools
  - OpenSTA
  - OpenTimer
  - Synopsys PrimeTime
  - Every timing driven tool has its own too
- We will cover this in depth.

Floorplanning

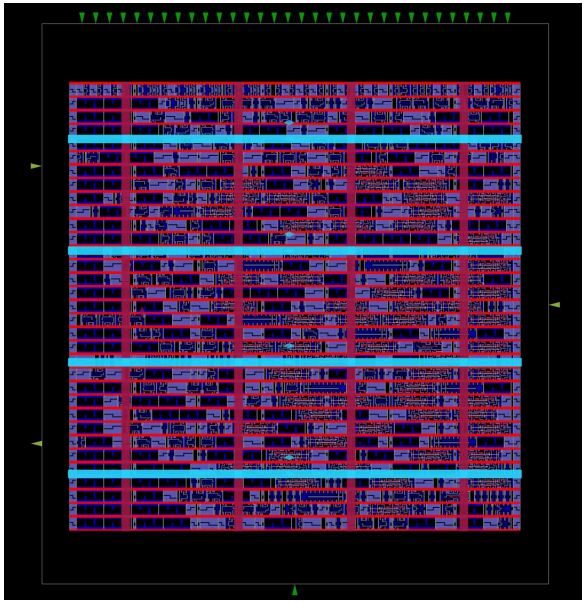
- Given: rough area of logic cells and modules from synthesis
- Define regions for “blocks” for each module
- Plan power network (based on power usage)
- Assign IO pins/pads (based on package)
- Common tools:
  - ParquetFP in OpenRoad
- We will cover this.

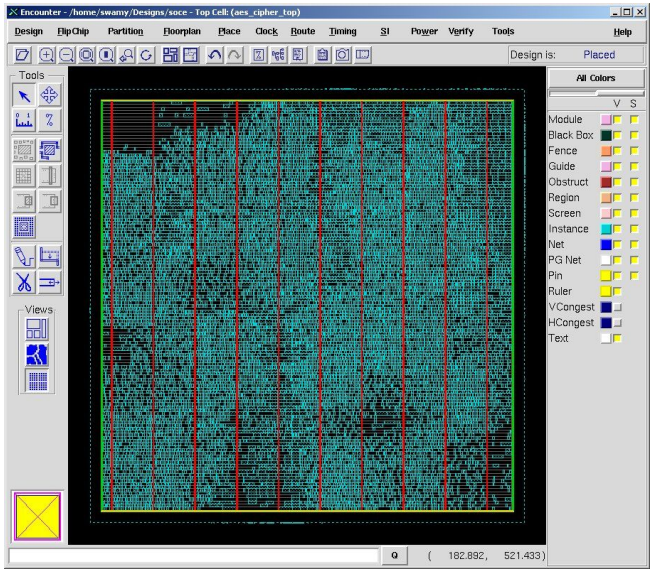




Placement

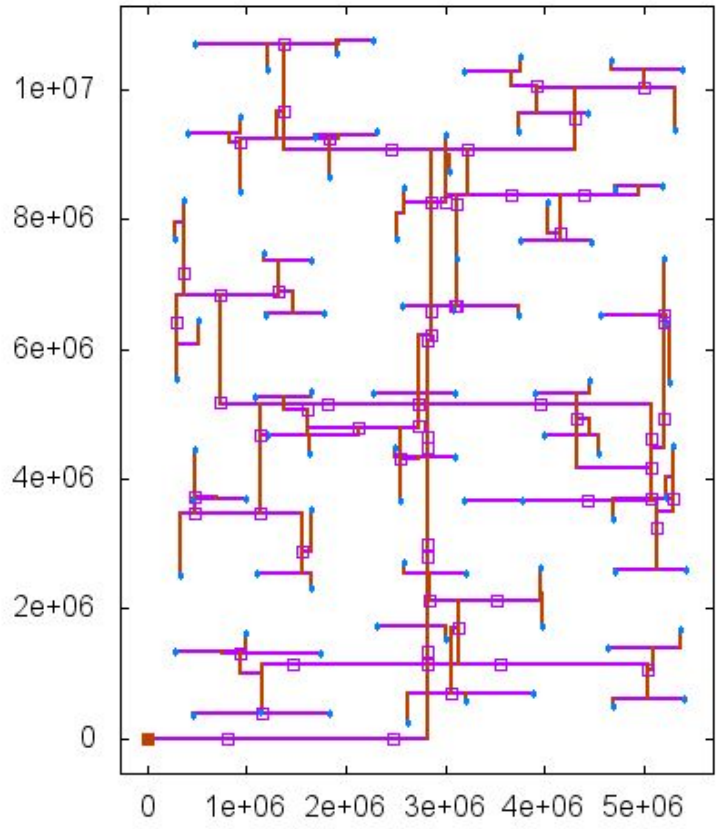
- Given “blocks” place library cells to minimize wire length or delay
  - For small designs, it is often “flat” placement
  - For large designs, each block is placed
- Iteratively partition, force directed, simulated annealing, etc.
- Common (academic) tools
  - RePlAce in OpenRoad
  - Capo by Michigan
  - FastPlace by Iowa State
  - Dragon by UCLA
- We will cover some of this.





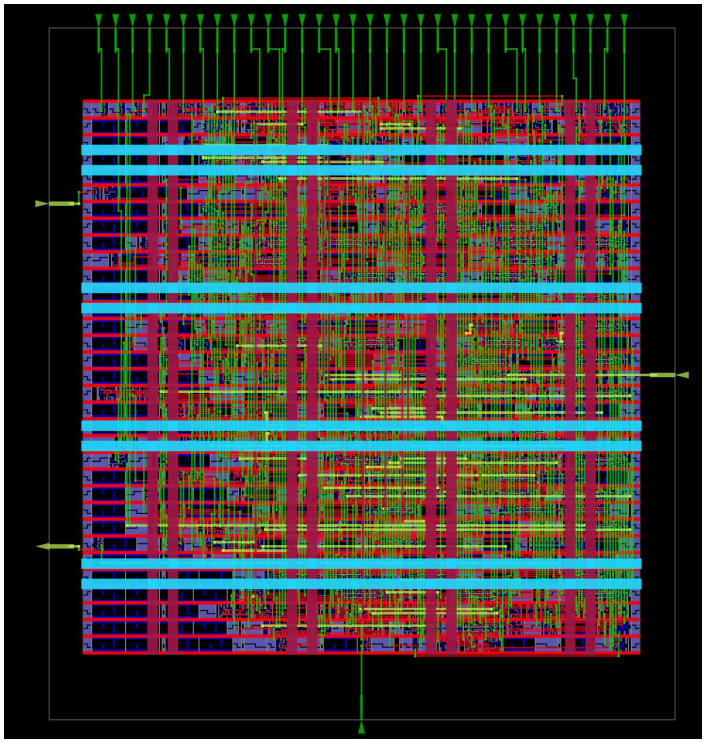
Clock Synthesis

- Place buffers (avoid blockages of standard cells)
- Route wires (on global layers)
- Minimize some function of
  - Skew
  - Power
  - Slew
  - Yield
- Common tools:
  - TritonCTS 2.0 in OpenRoad
  - CTGen by Cadence
- We will cover some of this.



Routing

- Route all other signals using preferred direction of each layer
- Global vs detailed routing
  - Global defines which regions a wire goes through
  - Detailed actually assigns layers and vias
- Buffer insertion
- Common tools:
  - FastRoute (OpenRoad global)
  - TritonRoute (OpenRoad detailed)
  - Cadence Nanoroute
  - BoxRouter by UT Austin
  - FGR by Michigan
  - Etc.
- We will cover some of this.

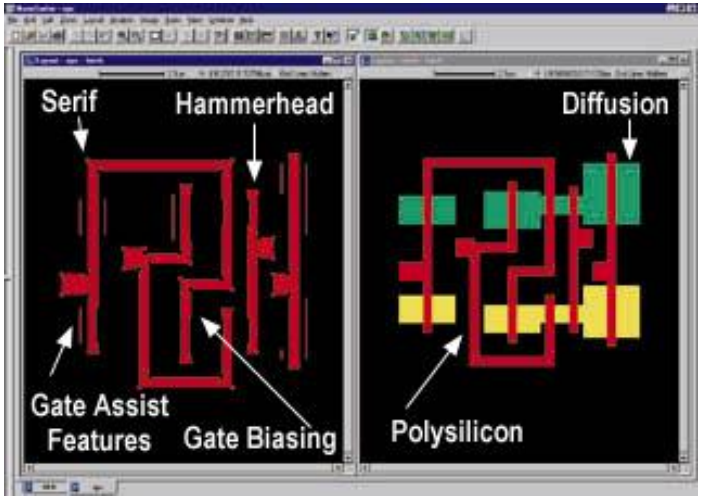


DRC/LVS

- Check that a design satisfies design rules for fab
- DRC often extracts netlist from layout too
- LVS compares design netlist with extracted netlist
- Often catches common errors
  - Power supply misconnection
  - Well connection errors
  - Bus flipped
  - IP design errors
  - Tool optimization errors!
- Common tools
  - Mentor Calibre
  - Netgen in OpenRoad
  - Magic in OpenRoad
- We will cover some of this.

OPC/RET

- Once physical layers are defined, OPC/RET improves printability
- Rule-based or model based
- Need to know adjacent cell information since proximity of shapes is important
- Requires long simulations and optimization
- Common tools:
  - Mentor OPCPro
  - Mentor nmOPC
- We will cover some of this.



Next

- Next topic: Fabrication